Symbolic Behavioral Modeling for Slew and Settling Analysis of Operational Amplifiers*

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***Abstract*—Traditionally symbolic techniques are used for analyzing small-signal circuit behaviors. They are not suitable for analyzing the large-signal transient responses of operational amplifiers (op-amps). This paper combines a symbolic dominant pole technique with a popular slew and settling analysis technique existing in the literature to form a symbolic transient analysis method which can be used for fast characterization of the op-amp behavior in the time-domain. A unified technique for slew and settling characterization is proposed. Experimental results have validated that the proposed method can calculate the slew and settling time of a two-stage op-amp more accurately for both large and small current designs.**

***Index Terms*—Operational amplifier, settling behavior, slew rate, symbolic analysis, transient response.**

I. Introduction

Two-stage operational amplifiers (op-amps) can provide flexible performance characteristics in dc gain, speed, and swing. When designing op-amps for power-efficient mixed-signal applications in data conversion, the settling performance optimization is an important design issue [1]. The large signal slewing and linear settling behavior determines the closed-loop response speed of operational amplifiers (see Fig. 1).

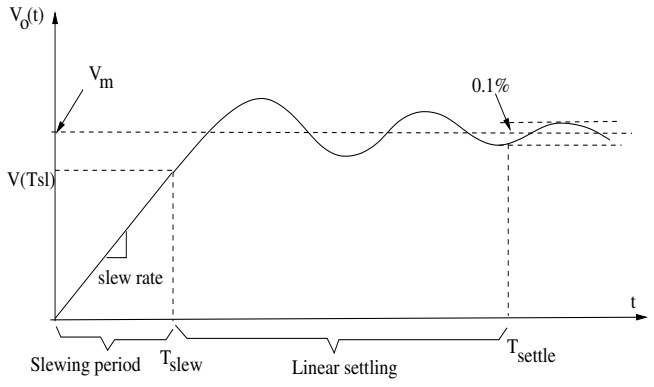

Fig. 1. Step response of an operational amplifier.

In 1982 C. T. Chuang proposed a second-order behavioral model for settle behavior analysis [2]. The behavioral model for a voltage follower configuration is shown in Fig. 2(a) as a feedback system consisting of a saturation component and a linear transfer block. In this model, when the output is in the slewing period, the available current of the input stage charging the compensation capacitor is *limited*, which can virtually be treated as if the feedback loop is opened. Thus the slewing period behavioral model operates in the open-loop mode as shown in Fig. 2(b). When the output voltage reaches the vicinity of its final value, the differential input stage enters the *linear region* and the feedback loop in the behavioral model is closed as shown in Fig. 2(c).

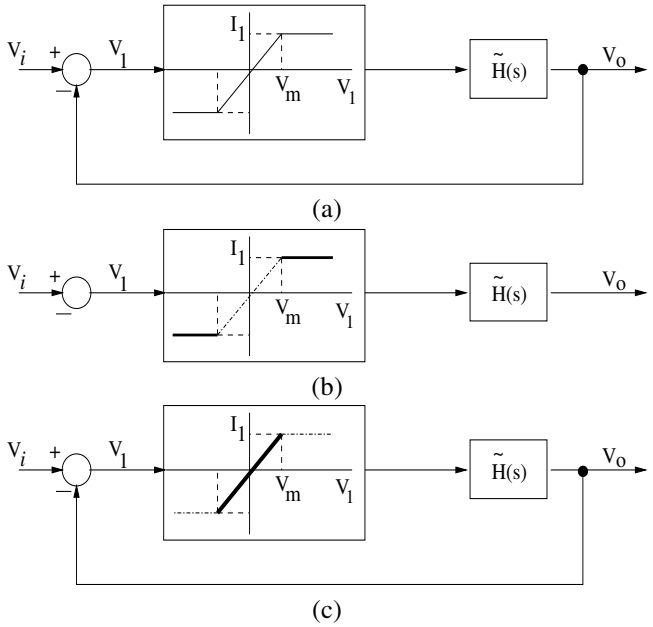

Fig. 2. (a) Op-amp behavioral model for transient analysis [2]. (b) Open-loop model for the slewing behavior with $|V_1| \geq V_m$. (c) Closed-loop model for the settling behavior with $|V_1| < V_m$.

Two key components necessary for determining a behavioral model as given in Fig. 2(a) are: 1) the charging current limit I_1; and 2) a two-pole transfer function $\widetilde{H}(s)$.

For the first component, Chuang [2] originally used a constant limiting current I_1 (see Fig. 3) for the slewing behavior analysis. But this assumption is not always valid in all applications, especially in emerging low-power applications. Yavari et al. [3] recently argued that for slew rate analysis the charging current should not be considered a constant. For example, the current flowing through the MOS transistor M4 in the nMOS-input Miller op-amp (Fig. 3) charges the compensation capacitor C_c. If the current in the output stage I_2

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is restricted for power constraint, the charging current would be the result of M4 *operating in the linear region*. Yavari et al. proposed a first-order model for predicting the slew rate [3]. Although this method provides an improved characterization of slew rate in low current designs, it is not able to predict the transient waveform including both the slewing and the settling periods.

For the second component, a *two-pole* linear transfer function $\widetilde{H}(s)$ was used by Chuang for modeling the linear small-signal settling behavior. The two poles were obtained by analyzing a simplified two-stage small-signal equivalent circuit in Chuang's work [2]. Given a design, Chuang used the same $\widetilde{H}(s)$ for modeling both the slewing and settling behaviors.

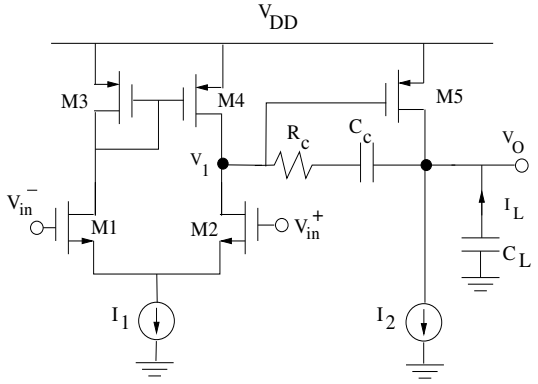

Fig. 3. Two-stage CMOS op-amp with nMOS input pair [3].

So far, the two methods have co-existed independently, one for large current applications (Chuang's model [2]) and the other for low current applications (Yavari's model [3]). This paper attempts to provide a unifying method that is applicable to a large extent of current variations with the same configuration of two-pole behavioral model. Moreover, a symbolic formulation is introduced so that the parametric behavioral model can provide transient waveforms efficiently for variational circuit parameters.

Unlike Chuang's model where the same $\widetilde{H}(s)$ is used for both phases of slewing and settling, we propose to use the two-pole model with different poles for each phase. The two sets of poles are extracted from two different biasing conditions; one for the slewing period and the other for the setting period. With a symbolic framework, we only need to construct two symbolic dominant poles once. Then the dominant poles corresponding to different biasing conditions can be computed by using the same symbolic construction. Hence, computational overhead is reduced. The poles extracted from small-signal analysis are believed to be more accurate than that obtained by an equivalent circuit analysis done by Chuang [2]. Furthermore, with symbolic analysis, for the first time we are able to create an explicit correspondence between the time-domain large-signal performance metrics and critical circuit parameters. With the availability of such a tool, laborious design tasks such as statistical (variational) performance analysis and design optimization in the time-domain can be made much easier.

II. Symbolic Dominant Pole Analysis

A rational transfer function can be expressed as follows:

$$H(s) = \frac{N(s)}{D(s)} = \frac{b_0 s^0 + b_1 s^1 + \cdots + b_q s^q}{a_0 s^0 + a_1 s^1 + \cdots + a_r s^r}, \qquad (1)$$

which is in *s-expanded* form. In symbolic ac analysis, a symbolic transfer function can be derived which can be either in *non-expanded* form or *s-expanded* form [4]. With an *s-expanded* form, the coefficients b_j's and a_k's in (1) are symbolic functions of small-signal circuit parameters.

In general it is hard to find the symbolic roots of a symbolic polynomial directly, although some approximation techniques have been studied [5], [6]. Different from these methods, there exists another approximation method which is computationally easier. We propose to use the *moment matching* technique [7], which can help to derive a few dominant roots symbolically.

The Taylor expansion of the transfer function $H(s)$ at $s = 0$ can be written in a series of s^k

$$H_{ex}(s) = m_0 s^0 + m_1 s^1 + m_2 s^2 + m_3 s^3 + \cdots, \qquad (2)$$

where the coefficients m_k's are called the *moments* [7]. By matching the coefficients of the expressions in (1) and (2); namely, $N(s) = H_{ex}(s)D(s)$, we get the following equations (assuming $a_0 \neq 0$, i.e., no pole at dc)

$$m_0 = \frac{b_0}{a_0} \qquad (3a)$$

$$m_1 = \frac{b_1 - m_0 a_1}{a_0} \qquad (3b)$$

$$m_2 = \frac{b_2 - m_0 a_2 - m_1 a_1}{a_0} \qquad (3c)$$

$$\cdots\cdots$$

Hence, if all the rational coefficients b_j's and a_k's are symbolic functions, we can obtain recursively the symbolic moments in terms of the circuit parameters. In application, we usually use low-order approximations, meaning that we only need to derive symbolic expressions of the few leading moments m_0, m_1, m_2, and m_3, etc.

Some symbolic simulators use binary decision diagrams (BDDs) for a compact representation of the symbolic network function $H(s)$ [8], [9], whose computational efficiency has been proven much higher than other methods. Those BDD-based methods also can derived s-expanded forms of $H(s)$ with the coefficients sharing the same BDD. As a result, the symbolic representations of the moments are compact as well.

The low-order symbolic moments can be used then to obtain symbolic expressions for a few low-order poles or zeros. For example, for the application addressed in this paper, it is sufficient to find the symbolic expressions for two dominant poles of an op-amp, p_1 and p_2, assumed distinct (i.e., $p_1 \neq p_2$). Assume that

$$\widetilde{H}(s) = \frac{k_1}{s - p_1} + \frac{k_2}{s - p_2} \qquad (4)$$

is a low-order approximation of the op-amp open-loop transfer function. The symbolic expressions for p_1 and p_2 are determined by *moment matching* as follows. Taylor expanding $\widetilde{H}(s)$ gives

$$\widetilde{H}_{ex}(s) = -\left(\frac{k_1}{p_1}+\frac{k_2}{p_2}\right)s^0 - \left(\frac{k_1}{p_1^2}+\frac{k_2}{p_2^2}\right)s^1 - \left(\frac{k_1}{p_1^3}+\frac{k_2}{p_2^3}\right)s^2 - \cdots \tag{5}$$

Equating the leading coefficients of (5) to that of (2), we get

$$p_1 + p_2 = \det\begin{vmatrix} m_1 & m_3 \\ m_0 & m_2 \end{vmatrix} / \det\begin{vmatrix} m_2 & m_3 \\ m_1 & m_2 \end{vmatrix}; \tag{6a}$$

$$p_1 p_2 = \det\begin{vmatrix} m_2 & m_1 \\ m_1 & m_0 \end{vmatrix} / \det\begin{vmatrix} m_2 & m_3 \\ m_1 & m_2 \end{vmatrix}. \tag{6b}$$

The above expressions indicate that the two dominant poles can be determined symbolically provided that the *symbolic moments* are available.

This paper proposes to use the two-pole model given in (4) for the behavioral linear block $\widetilde{H}(s)$ shown in Fig. 2(a). With symbolic expressions for the two dominant poles, re-computation of the poles becomes easier when the circuit bias conditions are altered.

III. Behavioral Slew and Settling Analysis

The slewing behavior is caused by the switching of the input signal from one voltage level V_1 to another V_2. While the second voltage level V_2 sustains, the circuit operates around the reference biasing given by V_2. Hence, we use the input level V_2 for a dc bias analysis which is used for obtaining the small-signal parameter values. These parameter values are used by our symbolic simulator to obtain the s-expanded symbolic $H(s)$ for the *settling phase*.

The trickier part is to determine the biasing condition at the switching instant which triggers the output slewing. During this period, it is hard to determine what biasing condition should be used for the small-signal parameter values characterizing the slew behavior. After a few testing, we found that the middle voltage level, i.e., $V_{0.5} := (V_1 + V_2)/2$ was a good reference biasing voltage at the input. The rest of the computation procedure remains the same as what we do for the settling analysis.

The behavioral transient analysis procedure can be summarized as follows:

Step 1. Given an op-amp circuit, use a symbolic circuit simulator to construct an s-expanded symbolic network function $H(s)$.

Step 2. Use the formulas given in (3) and (6) to obtain the symbolic expressions for the two dominant poles.

Step 3. Use the mid-voltage of two switching levels for the slew biasing and the final voltage for the settling biasing. Run SPICE dc analysis twice to get the two sets of small-signal parameter values.

Step 4. Use the symbolic poles to get the two sets of numerical poles. Obtain the transient waveform using the second-order model. Use the limiting current I_1 and the g_m of the input differential pair for the linear gain in the saturation component in both parts of behavioral computation.

IV. Experimental Results

The proposed behavioral slew and settling analysis method was tested on a few circuits. First we tested the accuracy of the proposed method for slew rate calculation and compared the result to that computed by the Yavari's method and HSPICE. The HSPICE results were considered golden. For the circuit shown in Fig. 3, same as that used in Yavari et al. [3], we calculated the slew rate using the proposed symbolic method for an input voltage applied at V_{in}^+ switching from high to low. The circuit parameters are given in Table I

Shown in Fig. 4 is the comparison result of the three methods. It is seen clearly that over the range of tested currents, the newly proposed method follows the accuracy of HSPICE, while the Yavari's model is valid only at low currents. This test demonstrates the our new behavioral model is able to characterize the slew behavior over a wider range of biasing conditions.

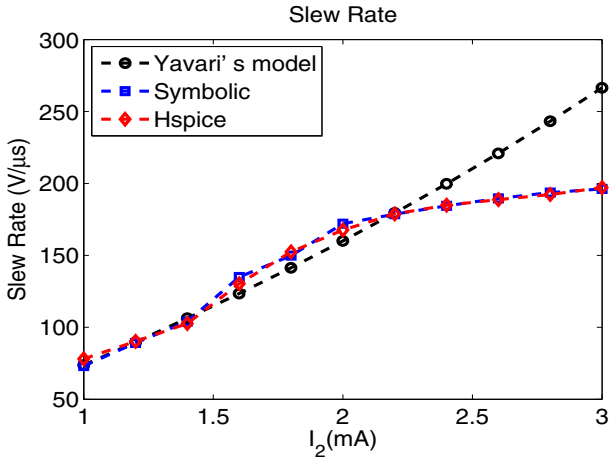

Fig. 4. Comparison of the slew rates computed by the three methods.

Next we report the tested results on the settling behavior and the overall step response waveform. The two-stage op-amp circuit with pMOS input pair given in Fig. 5 was used for this part of test. The circuit parameters are given in Table II. Shown in Fig. 6 is the comparison of the measured settling times using Chuang's model [2], our symbolic model, and the HSPICE result. It is clearly seen that our symbolic method provided a better settling time measurement (closer to the HSPICE result) than that obtained by Chuang's model for C_c varying from $5pf$ to $14pf$. A step response comparison is given in Fig. 7 to show the accuracy of the approximate transient responses predicted by Chuang's model and our symbolic model. The response curve by the symbolic model is much closer to the HSPICE response.

V. Conclusion

This paper has proposed a symbolic slew and settling characterization method for op-amp time-domain performance

TABLE I
CIRCUIT PARAMETERS USED FOR SLEW RATE TEST (TSMC 0.18μM TECHNOLOGY).

$(W/L)_{1,2}$	$(W/L)_{3,4}$	$(W/L)_5$	R_c	C_c	C_L	I_1	V_{DD}	Input
50/0.5	100/1	150/0.5	400 Ω	5pf	5pf	1mA	3V	2V → 1V

TABLE II
CIRCUIT PARAMETERS USED FOR SETTLING TEST (TSMC 0.18μM TECHNOLOGY).

$(W/L)_{1,2}$	$(W/L)_{3,4}$	$(W/L)_5$	$(W/L)_6$	$(W/L)_7$	$(W/L)_8$	R_c	C_c	C_L	I_S	V_{DD}	Input
96/0.5	5/0.5	20/0.5	6/0.5	25/0.5	44/0.5	4.11 $k\Omega$	8pf	9pf	15 μA	1.8V	0.3V → 1V

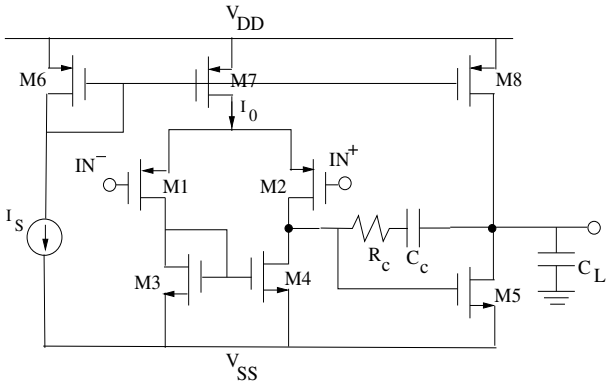

Fig. 5. Two-stage Miller op-amp with *p*MOS input pair.

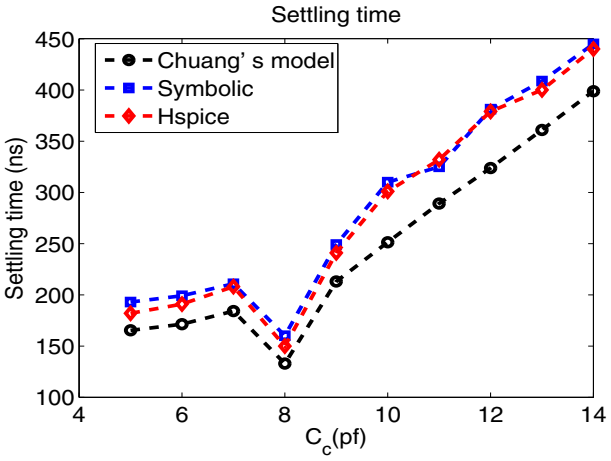

Fig. 6. Comparison of the settling times computed by the three methods with C_c varying over the range given.

analysis. The traditional two-pole model with a saturation component is extended to a symbolic formulation, where the two-pole model is obtained by moment matching. This novel extension turns out to be more accurate for both small current and large current applications. Experimental results have validated the effectiveness of the proposed method and its extended applicability. It is the first time that a symbolic analysis tool is applied for *large-signal* analysis in the time-domain.

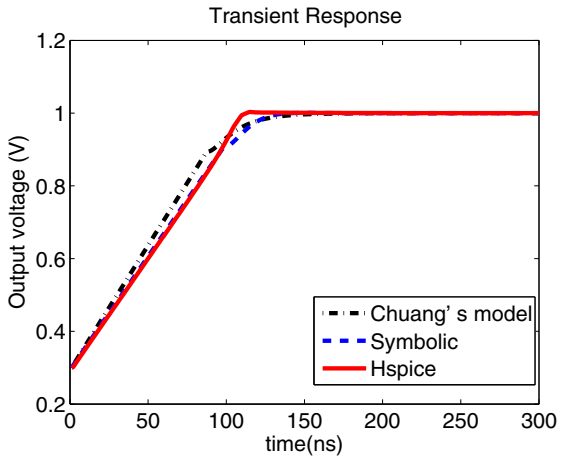

Fig. 7. Comparison of the step response curves computed by the three methods.

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