Lab #3: *Design a 8-bit Arithmetic Logic Unit*

8-bit Full Adder Design

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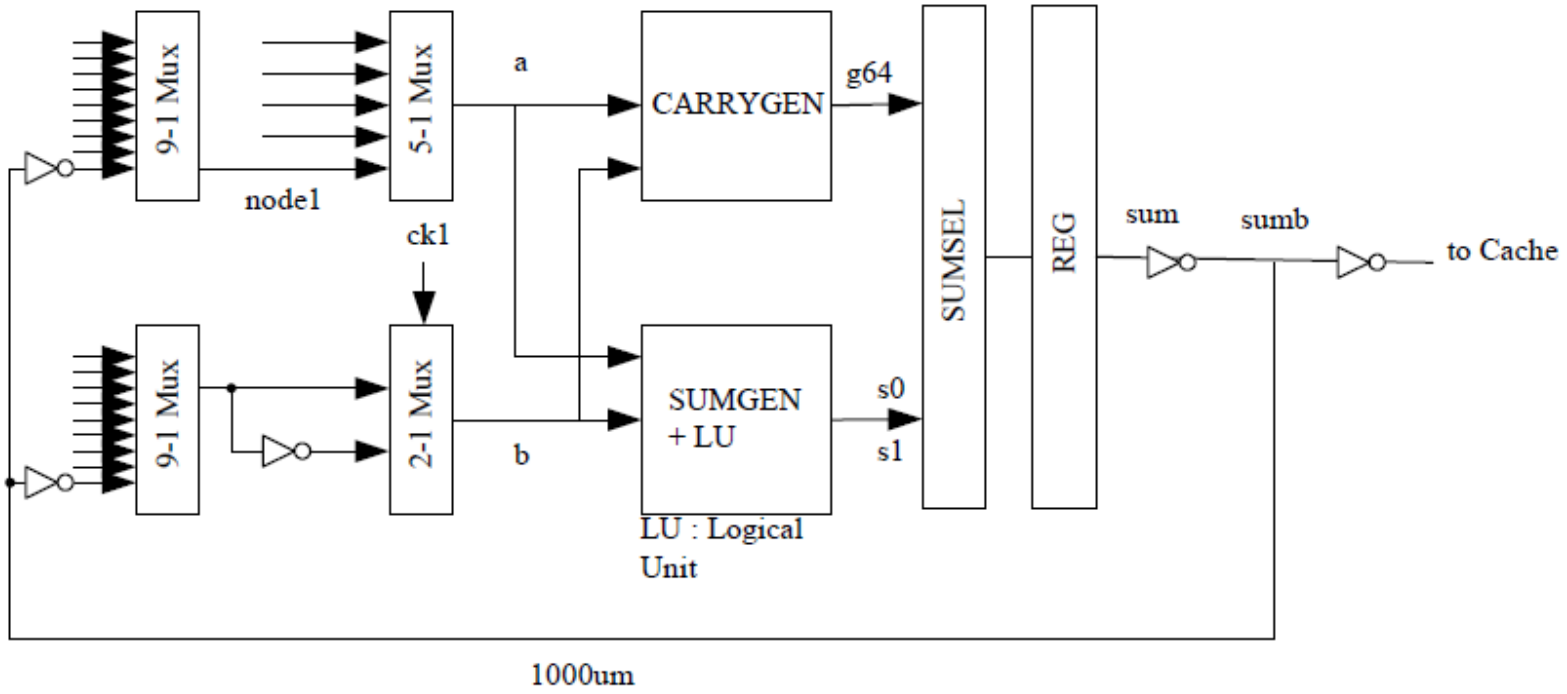
Outline

- Background
- Adder Design
- Lab3 Introduction
- Upload the Lab report

Background



Arithmetic-logic units are the heart of any microprocessor

Background

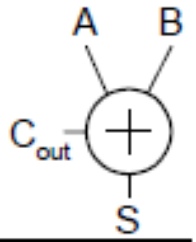
- An ALU has four major parts
  - Arithmetic block
  - Logic block
  - Multiplexers
  - Registers
- The core of the arithmetic block is an adder

Adder

Half Adder

$S = A \oplus B$

$C_{out} = A \cdot B$



A	B	C_{out}	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$S = A\overline{B}\overline{C} + \overline{A}B\overline{C} + \overline{A}\overline{B}C + ABC$

$= A \oplus B \oplus C = P \oplus C$

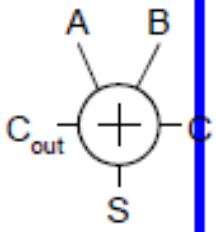
$C_{out} = AB + (A + B)C$

$= \overline{\overline{AB} + (\overline{A} + \overline{B})\overline{C}} = MAJ(A, B, C)$

Full Adder

$S = A \oplus B \oplus C$

$C_{out} = MAJ(A, B, C)$



A	B	C	C_{out}	S	
0	0	0	0	0	delete
0	0	1	0	1	
0	1	0	0	1	propagate
0	1	1	1	0	
1	0	0	0	1	
1	0	1	1	0	
1	1	0	1	0	generate
1	1	1	1	1	

PGK

- For a full adder, define what happens to carries
  - Generate: C_{out} = 1 independent of C
    - G = A • B
  - Propagate: C_{out} = C
    - P = A ⊕ B
  - Kill: C_{out} = 0 independent of C
    - K = ~A • ~B

$$C_o(G,P) = G + PC_i$$

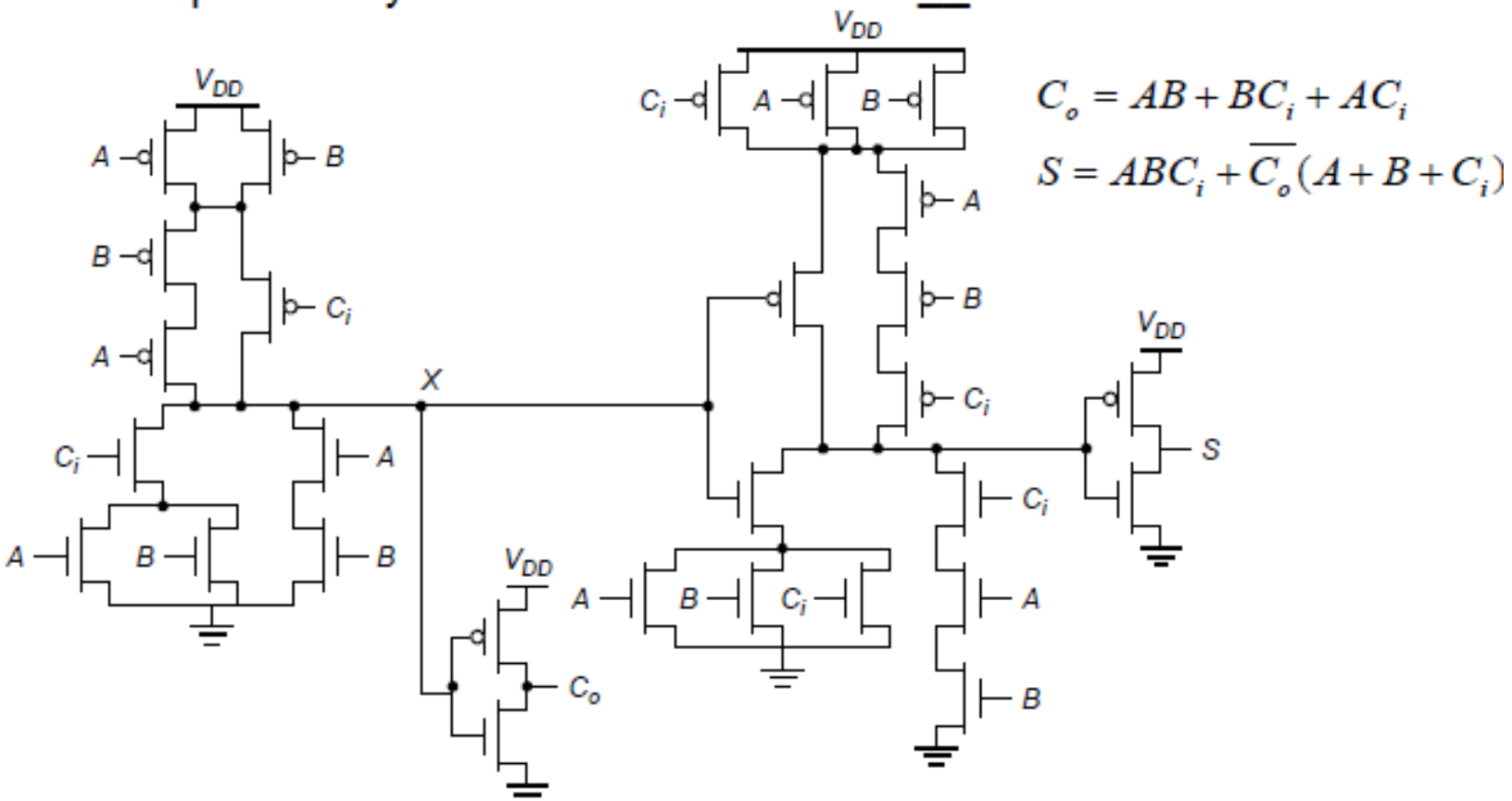
$$S(G,P) = P \oplus C_i$$

- Note that we will be sometimes using an alternate definition for

Propagate (P) = A + B

Full Adder Design-typical

Complimentary Static CMOS Full Adder__28 Transistors



Multi-bit Full Adder Design

- Carry-Ripple Adder
- Carry-Skip Adder
- Carry-Lookahead Adder
- Carry-Select Adder
- Tree Adder

Carry-Ripple Adder

- A N-bit full adder can be composed of N 1-bit full adder
- Critical path delay

$$t_{adder} \square (N-1)t_{carry} + t_{sum}$$

- CRA is not suite for long-word addition due to its propagation delay

Lab3 Introduction

Introduction

- Object:
  - Design a 8-bit Full Adder for a 8-bit ALU
- You can select any full adder structure and implement it with any circuit family:
  - Complementary Static CMOS
  - Pass-Transistor
  - Dynamic

Design Flow

- 1. Determine the FA structure
  - Carry-Ripple Adder(basic)
- 2. Determine circuit family
  - Complementary Static CMOS
  - Pass-Transistor
  - Dynamic
- 3. Design the full adder
  - Single-bit adder(Schematic/MOS size)
  - Multi-bit adder(Symbol)

Design Flow(cont')

- 4. Simulation
  - Functionality
  - Performance(Delay, power, EDP)
- 5. Optimize the performance
  - Size optimization
  - Structure optimization

LAB Requirements

- Basic Part
  - Design a 8-bit carry-ripple adder with any circuit family
  - Verify it and report the performance of your design, including delay, EDP, area(# of transistors)

LAB Requirements

- Optional part: Tasks
  - Design your full adder with other circuit families and compare the performance metric EDP by the possible methods:
    - Insert the buffers to optimize the stages and transistors size for a smaller transmission latency
    - Reduce the Vdd to decrease the power consumption
    - Combine the structure with other circuit families…
- You can choose one or more ways to finish if you have enough time

Tips

- log018.scs
  - Vdd 1.8V
  - MOS L 180nm
- unit
  - Time eg: input 3n, not 3ns
  - Cap eg: input 25f, not 25fF
- Model Name:
  - NMOS -- nchPMOS -- pch

Report Requirements

- Your lab report should include:
  - Circuit schematic of your design, including your transistor size(you may need to create symbols for your sub-circuits)
  - Your patterns to verify the full adder and corresponding performance index(Delay, power, EDP)

Report Submit

- Submit a pdf or word document with name lab3_adder_id_name, eg: lab3_adder_511…._zhanghua.pdf

- Upload it to MOODLE system no later than 23:55AM, June 16, 2013(two weeks)

Reference

- **Jan M. etc, *Digital Integrated Circuits: A Design Perspective, Second Edition***

Let’s Start!