Lab 1: HSPICE Simulation

1. Objective

The objective of this lab is to give students an initial exposure to the simulation program (HSPICE) that will be used in this course. Students will learn basic procedures for using HSPICE (netlist simulator) and Awaves (waveform analyzer). Students should have some basic knowledge on Unix/Linus OS commands. An Hspice tutorial will be provided with this lab manual.

This lab has two parts. In the first part you simulate one single NMOS transistor working as an inverter. In the second part you modify the netlist for the single NMOS inverter into a CMOS inverter and study the voltage transfer characteristics (VTC) by changing the channel width of the PMOS transistor.

2. Tasks

a) (Important!) Read Hspice tutorial at least once before you come to lab.

b) Follow TA's instructions to familiarize your computer and Unix commands.

c) Create a Spice netlist file named "nmos_inverter.sp" for the NMOS inverter shown in Figure 1. The netlist file contains the description of a RTL (Resistor Transistor Logic) inverter.
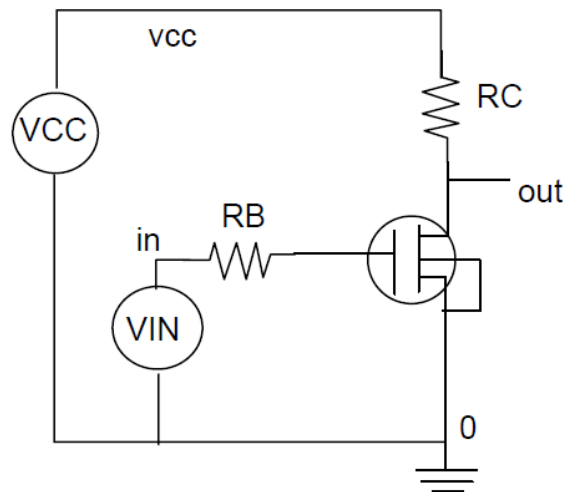

Figure 1. NMOS resistor inverter.

"nmos_inverter.sp"

```
Simple NMOS Inverter

.lib './cmos25.lib' TT

*netlist--------------------------------------

VCC vcc 0 5
VIN in 0 PULSE 0 5 2NS 2NS 2NS 30NS 70NS

RB in base 10k
M1 out base 0 0 NMOS L=0.5u W=10u

RC vcc out 1k

*extra control information--------------------

.options post=2 nomod
.op

*analysis-------------------------------------

.TRAN 1ns 300ns
.DC VIN 0 5 0.1

.END
```

There are three main sections in the spice netlist:
- The netlist description. Netlist is a description of the circuit schematic in a text file.
- The models used. A model in Spice is a description of the parameters of the equations used by Spice to analyze the circuit.
- The analysis to be performed during the simulation. In this netlist we request a transient analysis and the DC Transfer Characteristic of the circuit.

The statement .options post=2 is to output the plot in ascii (output file [netlist_name].sw#).

PART I:

d) Simulate the circuit netlist.
- Open Hspui from Hspice
- Click the "simulate" button in the visible window
- View the output result files
  - filename.sw0 is the DC sweep data output. (used by awaves)
  - filename.tr0 is the transient data output. (used by awaves)
  - filename.out is the output listing from HSPICE. (look here for simulation errors)
  - filename.st0 is the simulation run information. (not useful)
  - filename.ic is the information about input to HSPICE (not useful)

- View the result of the transient analysis via clicking "avanwaves" button

PART II:

In this part of lab, you modify the first netlist by replacing the resistor RC by a PMOS transistor connected as shown in Fig. 2. You will do the following:

1) Copy the previous netlist file "nmos_inverter.sp" to another file "cmos_inverter.sp".

2) Modify the netlist to describe the circuit shown in Fig. 2. For example, you'll add the next line in your new netlist:

M2 out base vdd vdd PMOS L=0.5u W=10u

3) Simulate this netlist once again and view the DC waveform in voltage transfer form.

4) Increase the channel width of the PMOS transistor by trying W=20u, 30u, 40u, etc. and simulate for each channel width. Write down what you observe from the VTC as you increase the width.

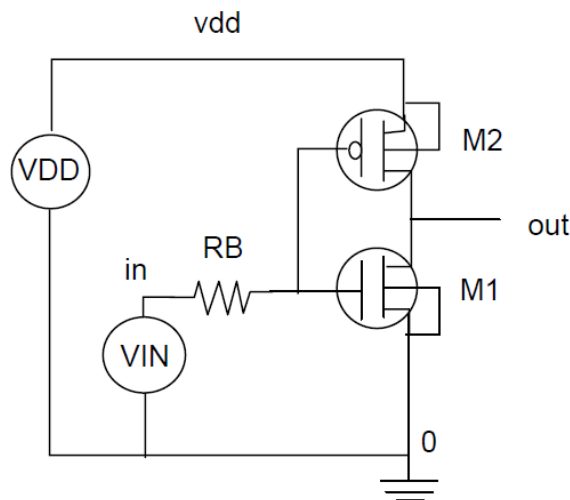M2 out base vdd vdd PMOS L=0.5u W=10u

Figure 2. CMOS inverter.

3. Lab Report

Write your lab report like writing a technical document. Always think about whether another person can easily understand what you write.

Your report must include an introduction of the background, your lab procedures, lab results, result analysis, and a conclusion. In your conclusion, add some comments on whether this lab is helpful to your understanding of the class material.

For this lab report you must include the following:

- A printout of the SPICE input files;

- Plots of the transient response of the circuits you have simulated;

- Plots of the DC transfer characteristic of the inverters.

Enjoy the lab!

Turn in your lab report(lab1_id_name.pdf) no later than next Saturday via Moodle.