上海交通大學 SHANGHAI JIAO TONG UNIVERSITY

电子信息与电气工程学院 School of Electronic Information and Electrical Engineering

微纳电子学系 DEPARTMENT OF MICRO/NANO ELECTRONICS

学 术 报 告 会

Seminar Announcement

题　目：Nano-Material Engineered Interconnect Technologies for Heterogeneous System Integration

日　期：2018-4-2（周一）上午 10:00-11:30

地　址：微电子楼401会议室

报 告 人：Prof. Mansun Chan
IEEE Fellow

Abstract:

The scaling of CMOS has encountered many hurdles in the sub-10nm technology nodes as we are approaching the end of the Moore's Law. The performance limitations have shifted to the interconnect technology to reduce the metal wire resistance as well as the k-value of the interlayer dielectrics. The popular interconnect materials such as copper and tungsten have been found to be insufficient due to increasing resistivity with dimension scaling and electromigration concern under high current density. And using porous structures to form the interlayer dielectrics is subjected to the weakening of the mechanical strength of the dielectric film. New materials such as carbon nanotube (CNT) and graphene have been extensively studied to extend the scaling roadmap for interconnects. However, many barriers have to be overcome before these materials can enter mainstream manufacturing. In this presentation, I am going to present some of the recent progresses in using CNT as a contact plug as well as an agent to form very low k-value interlayer dielectrics.

Biography:

Prof. Mansun Chan was one of the major contributors to the unified BSIM model for SPICE, which has been accepted by most US companies and the Compact Model Council (CMC) as the first industrial standard MOSFET model. Subsequently, he joined the Electrical and Electronic Engineering Department at Hong Kong University of Science and Technology. His research interests include emerging nano-device technologies, 2-D device for flexible electronics, Artificial Neural Network devices and applications, new-generation memory technology, BioNEMS, device modeling and ultra-low power circuit techniques. He is currently still consulting on the development of the next generation compact models.

Prof. Mansun Chan was a Board of Governor, Chair of the Education Committee, the Chair of the Region 10 subcommittee and a Distinguished lecturer of the IEEE Electron Device Society. In addition, he has received many awards including the UC Regents Fellowship, Golden Keys Scholarship for Academic Excellence, SRC Inventor Recognition Award, Rockwell Research Fellowship, R&D 100 award (for the BSIM3v3 project), IEEE EDS Education Award, Distinguished Teaching Award, the Shenzhen Science and Technology Innovation awards etc. He is a Fellow of HKIE, IET and IEEE.