



Chater 6 (II)

Dynamic Response of BJT

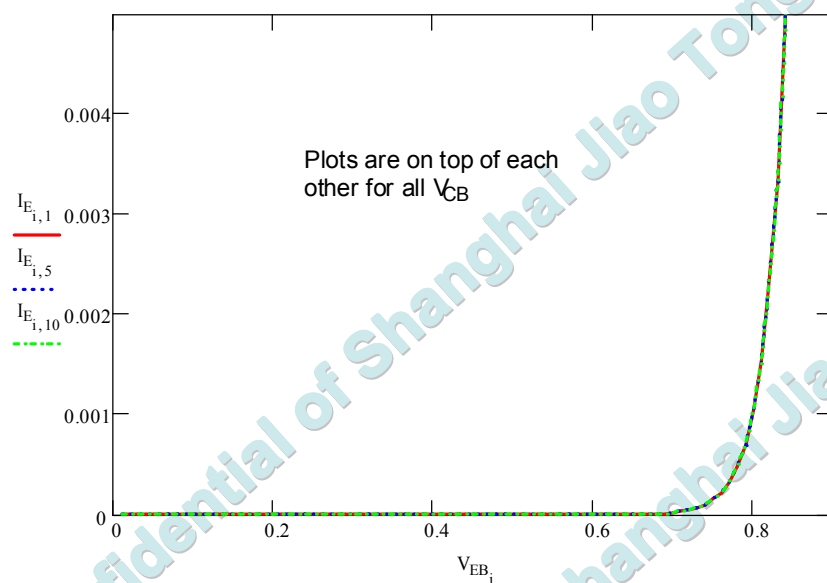
Xiulan Cheng/Shirla Cheng

2012-05-20

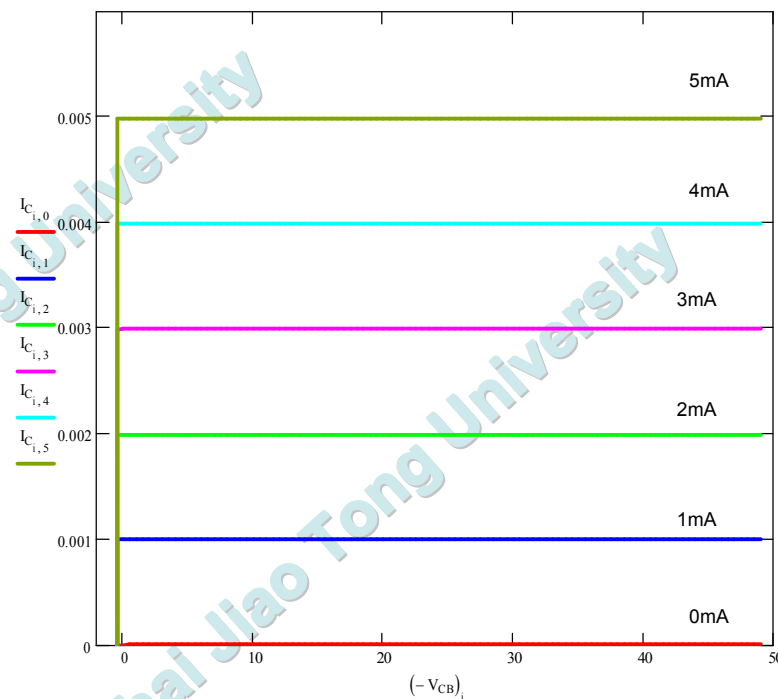




Common Base Characteristics



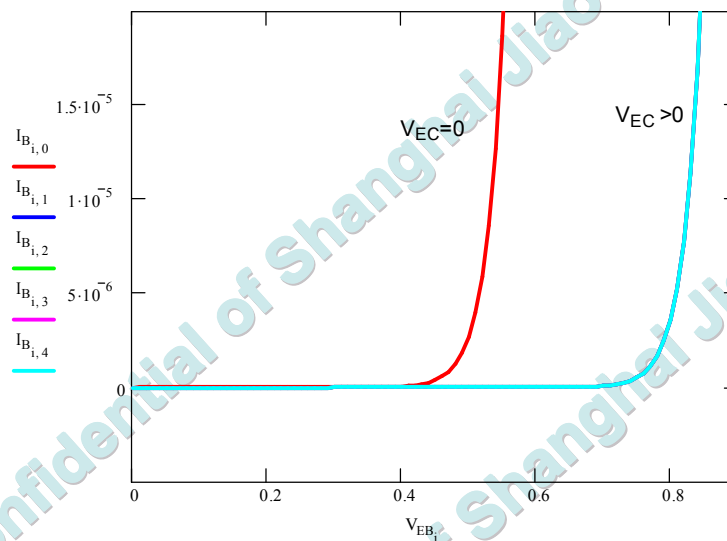
Input



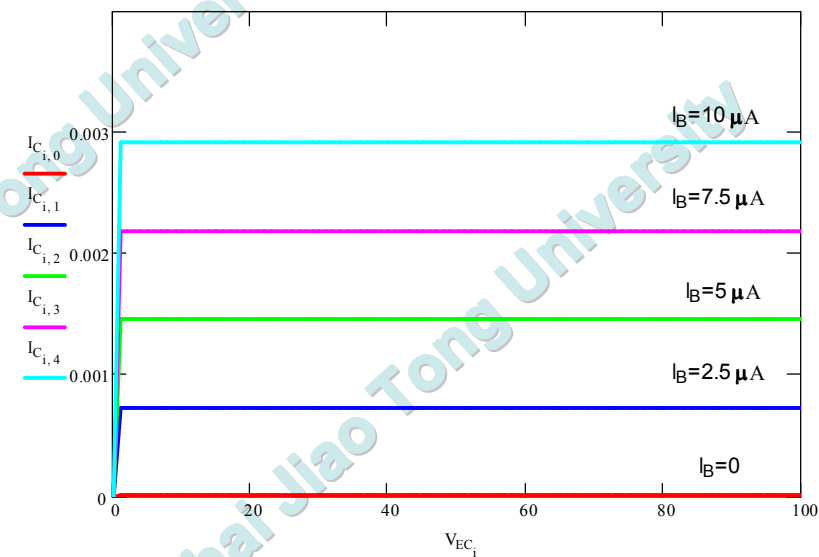
Output



Common Emitter Characteristics



Input
(Forward Biased
PN junction)



Output
(Reverse biased
PN junction ..
 I_s controlled by I_B)



Plans

- How do the computed BJT I-Vs compare with expts?
- Can we understand the discrepancies?
- What does the gain look like?
- AC properties (small signal and transient response)

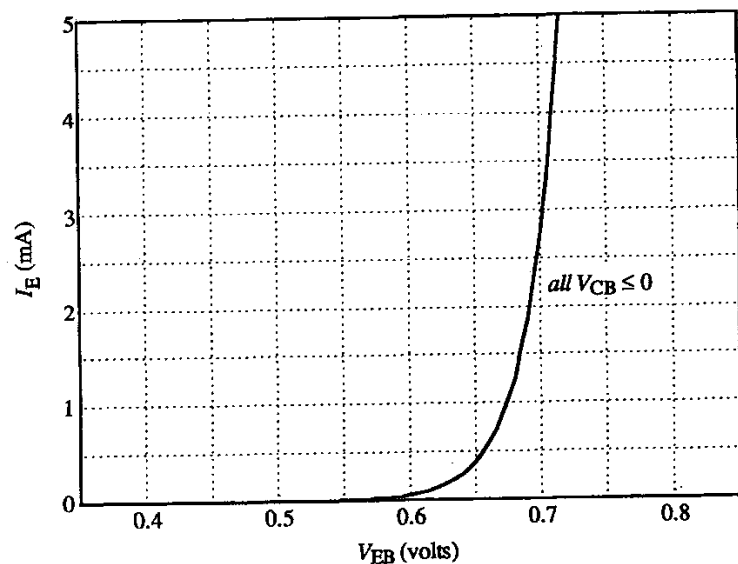


Common Base

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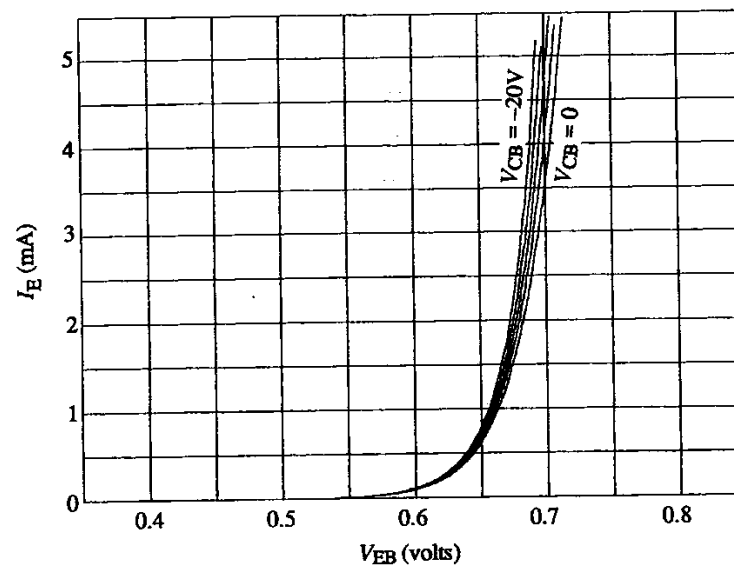
ELECTRONICS

THEORY

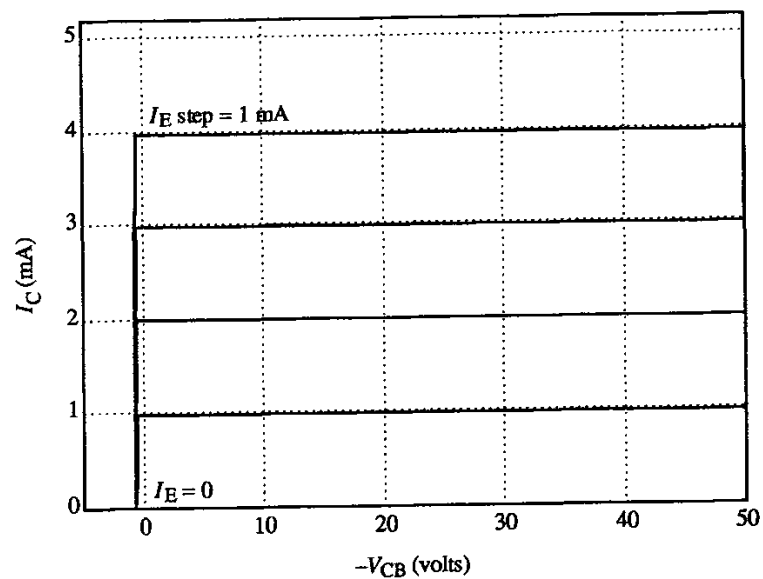


(a)

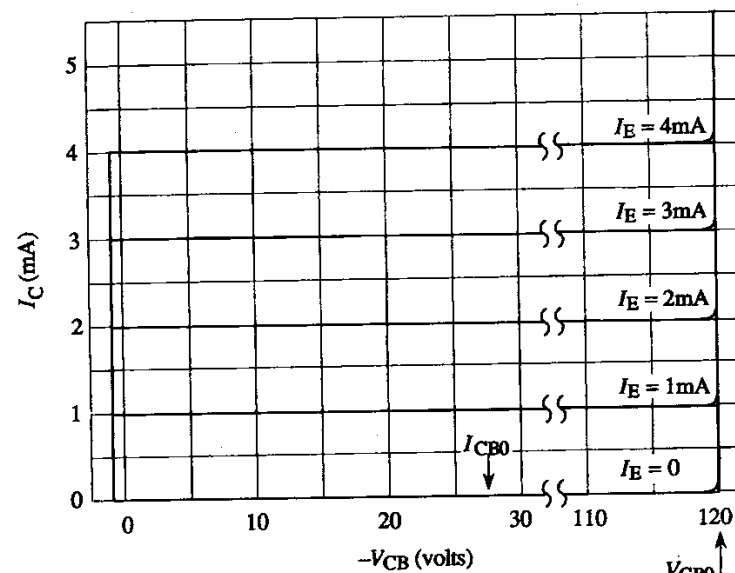
EXPERIMENT



(b)



(c)



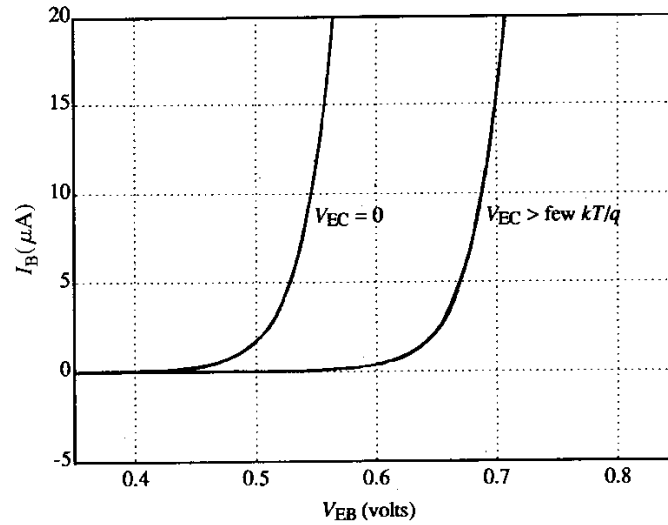
(d)



Common Emitter

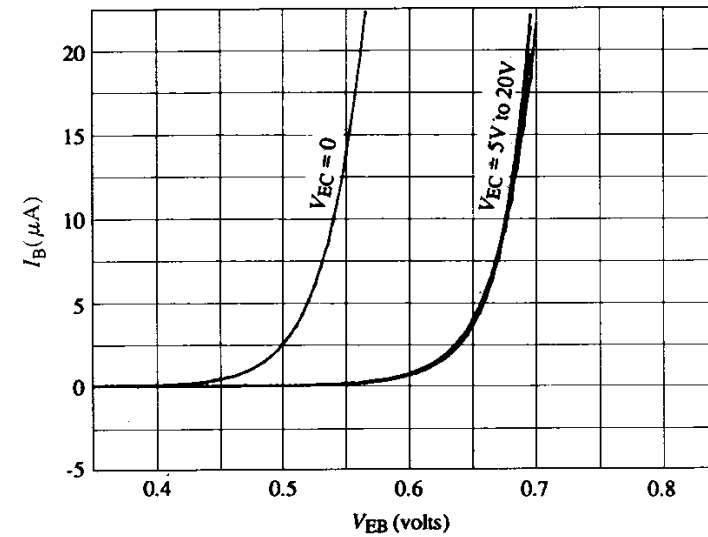
学院
ELECTRONICS

THEORY

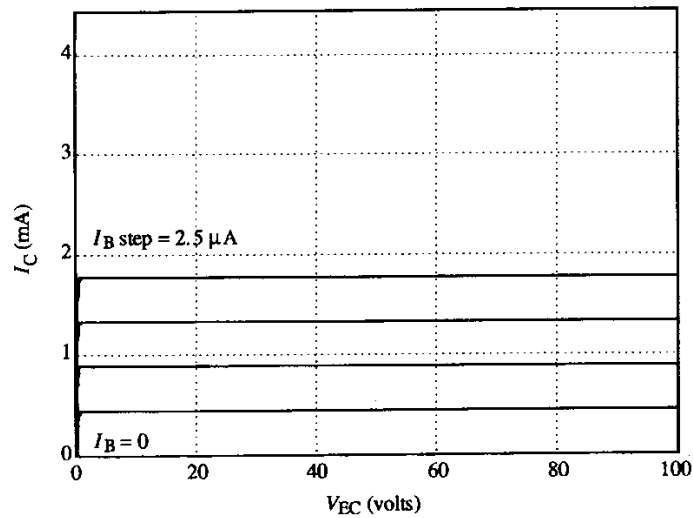


(a)

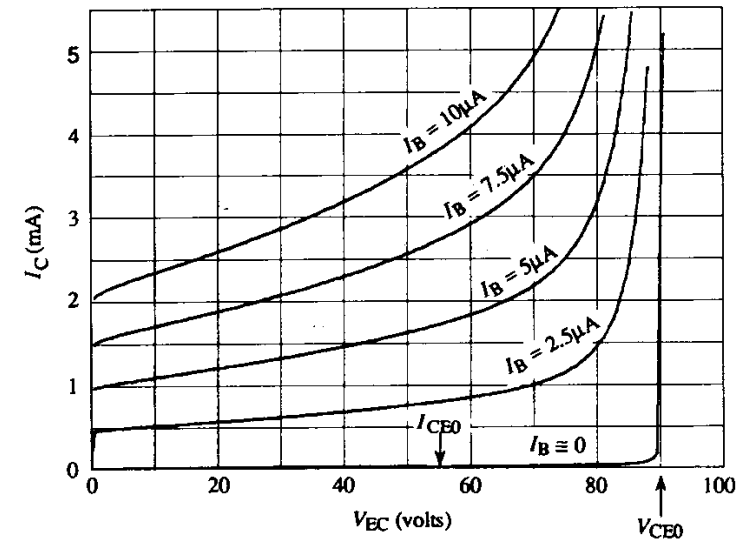
EXPERIMENT



(b)



(c)



(d)



What's wrong with these pictures?

Common Base:

- Input characteristic shows V_{CB} dependence
- Output shows breakdown at V_{CBO}

Common Emitter

- Input characteristic pretty good agreement
- Output characteristic:

- Upward slope in I_C - quasilinear V_{EC} dependence

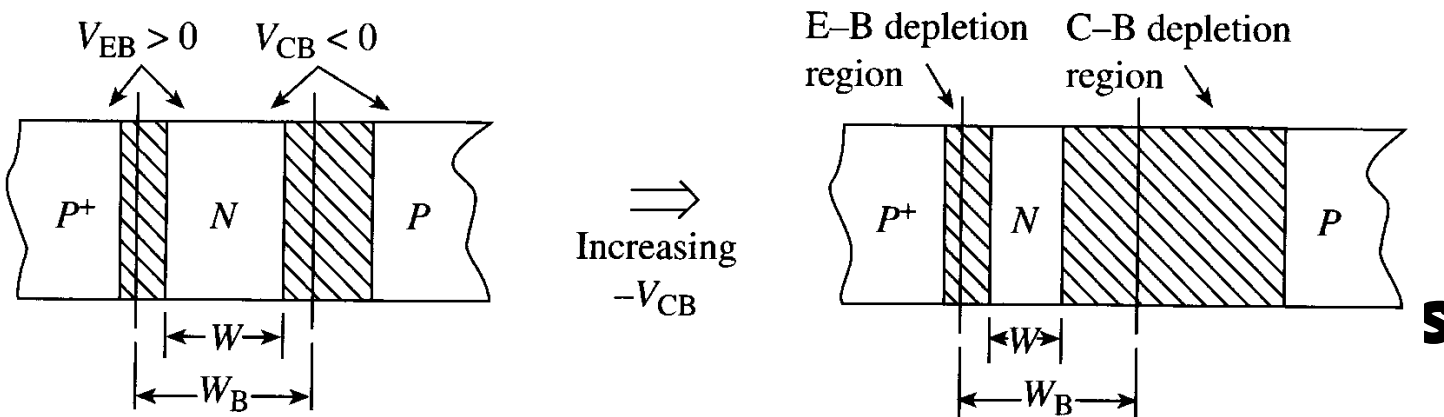
- Breakdown at V_{CEO}

- Upturn prior to breakdown



Base width has been assumed to be constant

When bias voltages change, depletion widths change and the effective base width will be a function of the bias



junction

Base width gets smaller as applied voltages get larger



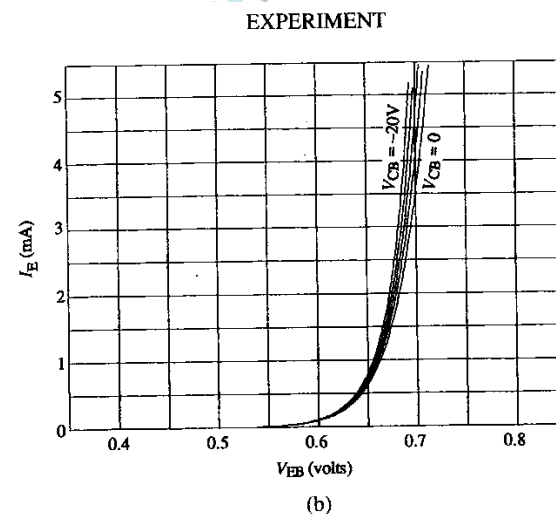
Early Effect: Common Base Input Characteristic

$$I_E = I_{F0} (e^{qV_{EB}/kT} - 1) - \alpha_R I_{R0} (e^{qV_{CB}/kT} - 1) \quad \text{Ebers-Moll}$$

Assuming $-V_{CB} > \text{few } kT/q$ and $W/L_B \ll 1$

$$I_{F0} \equiv qA \left(\frac{D_E}{L_E} n_{E0} + \frac{D_B}{L_B} p_{B0} \frac{\cosh\left(\frac{W}{L_B}\right)}{\sinh\left(\frac{W}{L_B}\right)} \right) \cong qA \frac{D_B}{W} p_{B0}$$

$$I_E \cong I_{F0} e^{qV_{EB}/kT} = qA \frac{D_B}{W} p_{B0} e^{qV_{EB}/kT}$$



Exponential prefactor will increase as V_{CB} increases (W decreases)



Early Effect: Common Emitter Output Characteristic

$$I_C = \beta_{dc} I_B + I_{CE0}$$
$$\beta_{dc} = \frac{1}{\frac{D_E W N_B}{D_B L_E N_E} + \frac{1}{2} \left(\frac{W}{L_B} \right)^2}$$

$$W_{eff} = W - W_{EB}|_{Base} - W_{CB}|_{Base} \cong W - W_{CB}|_{Base}$$

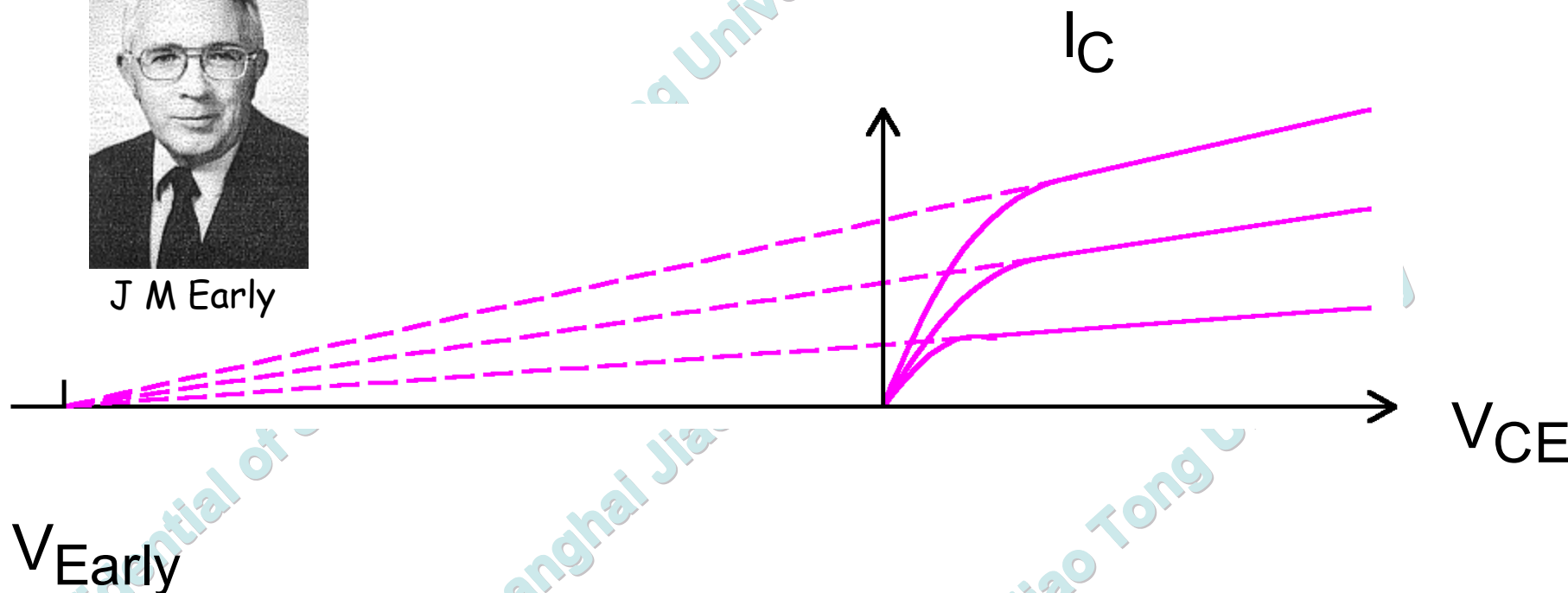
$$W_{CB} = \left[\frac{2K_S \epsilon_0 (N_A + N_D)}{q N_D N_A} (V_{bi} - V_{CB}) \right]^{1/2}$$

$$W_{CB}|_{Base} = x_n = W|_{Base} \left(\frac{N_C}{N_C + N_B} \right)$$

■ If $N_C \ll N_B$ most of the depletion is in the collector and modulation of base width is minimized - reduced Early Effect



J M Early



Converge ~ at single point called "Early Voltage" (after James Early)

Large "Early Voltage" = Absence of "Base Width Modulation"

= Transistor ~ immune to operating voltage changes

BUT requires wide base => lower gain



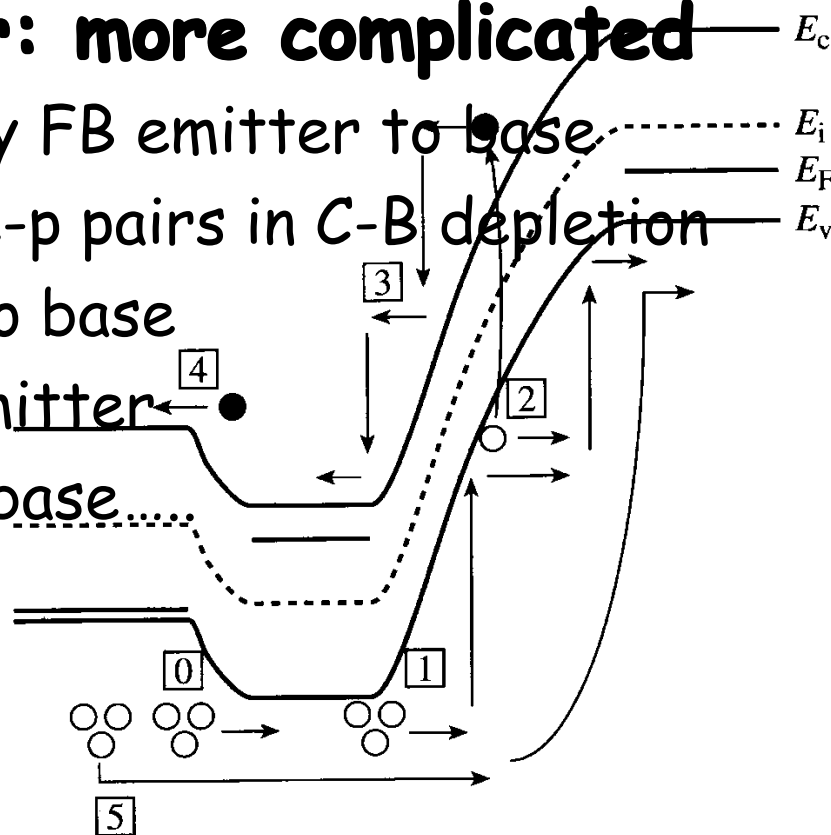
Avalanche

Multiplication

Common Base: Similar to single p-n junction $V_{CBO} \approx V_{BD}(B-C)$

Common Emitter: more complicated

1. holes injected by FB emitter to base
2. holes generate e-p pairs in C-B depletion
3. e- drift back into base
4. e- injected to emitter
5. more holes into base





Avalanche Breakdown: Common Emitter

$$I_C = \beta_{dc} I_B + I_{CB0} \rightarrow \frac{M \alpha_{dc}}{1 - M \alpha_{dc}} I_B + \frac{I_{CB0}}{1 - M \alpha_{dc}}$$

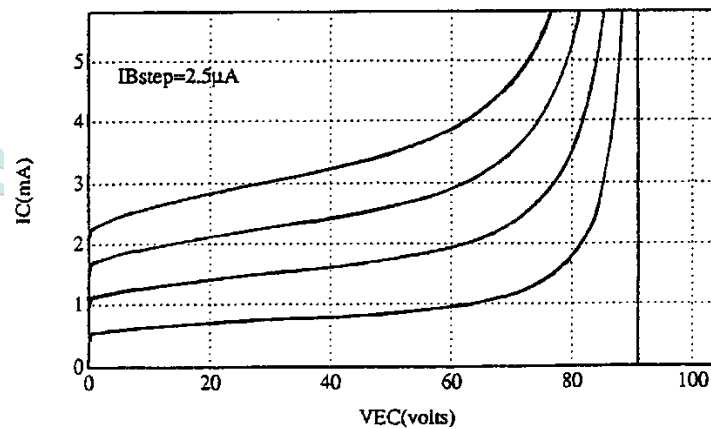
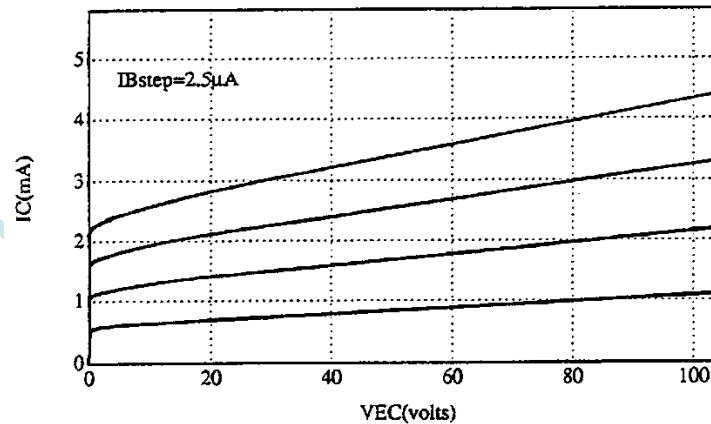
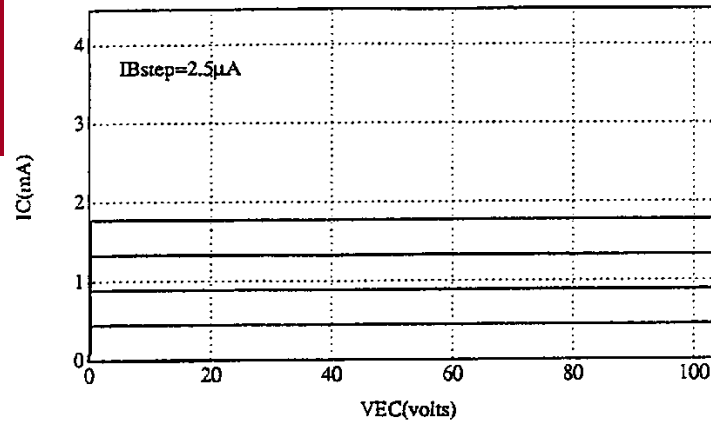
❏ $I_C \rightarrow \infty$ when $M \rightarrow 1/\alpha_{dc}$

❏ M only needs to be slightly greater than unity

ECE 663 ❏ $V_{CEO} < V_{CB0}$ – Breakdown voltage is lower for common Emitter mode than common



Ideal



W/base width mod
Early Effect

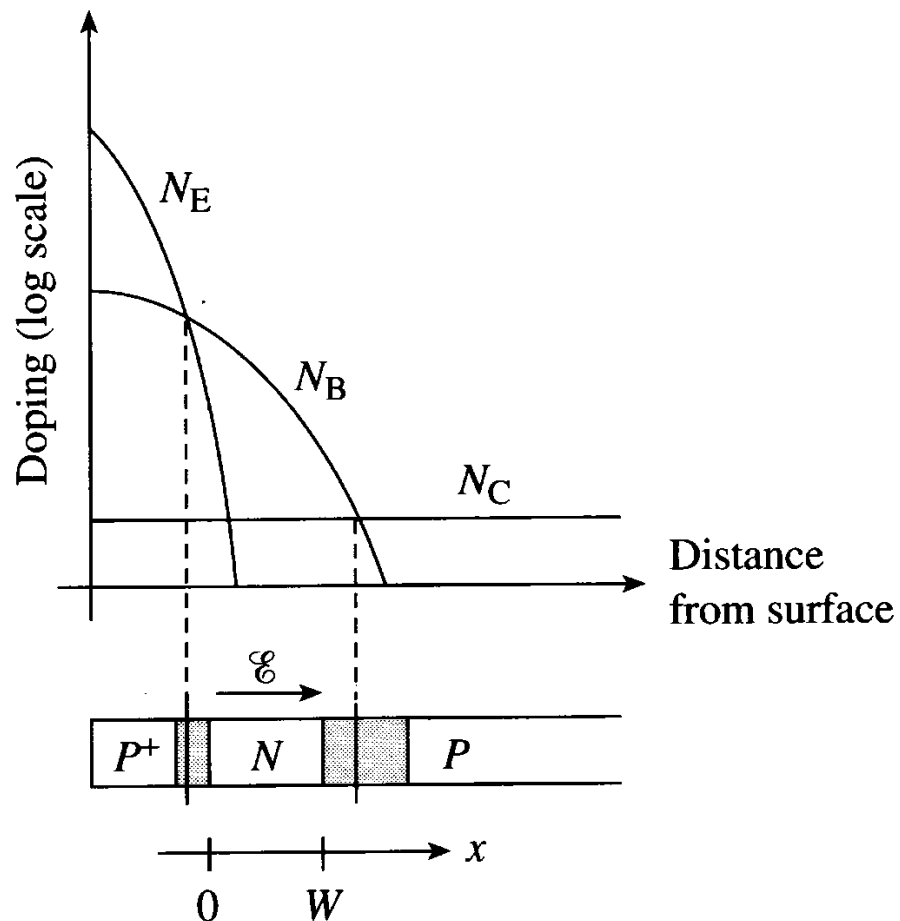
W/base width mod
& avalanche
multiplication



How can we mitigate these effects?



Graded Base



- Implant or diffusion leads to doping profile
- Doping profile leads to E field
- If Emitter is on top layer - E field acts to push carriers toward the collector
- Improved speed if limited by base transport time

$$E = -\frac{kT}{q} \frac{1}{N_B(x)} \frac{dN_B(x)}{dx}$$



Si-Ge HBT's for BiCMOS

❑ Dilemma for bipolar transistors:

- ❑ For high frequency operation want low base resistance - high base doping
- ❑ For high current gain want to minimize hole injection into emitter (nnp) - low base doping

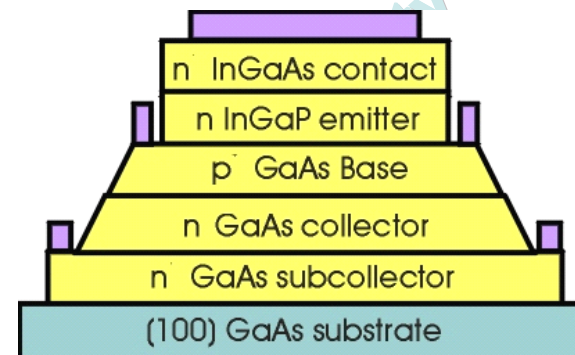
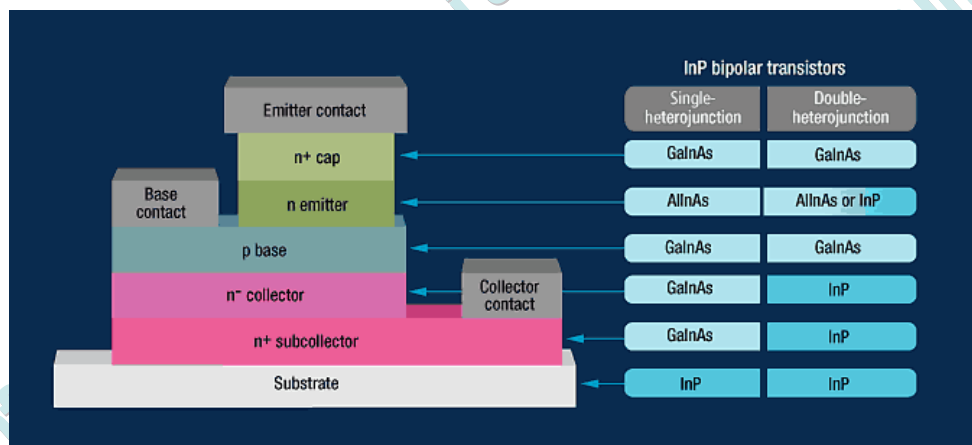
❑ Solution HBT – heterojunction bipolar transistors

❑ For CMOS integration use $\text{Si}_{1-x}\text{Ge}_x$ system

- ❑ Bandgap difference (1.12 eV Si, 1.0 eV, $\text{Si}_{0.8}\text{Ge}_{0.2}$)
- ❑ 80% ΔE_c in VB

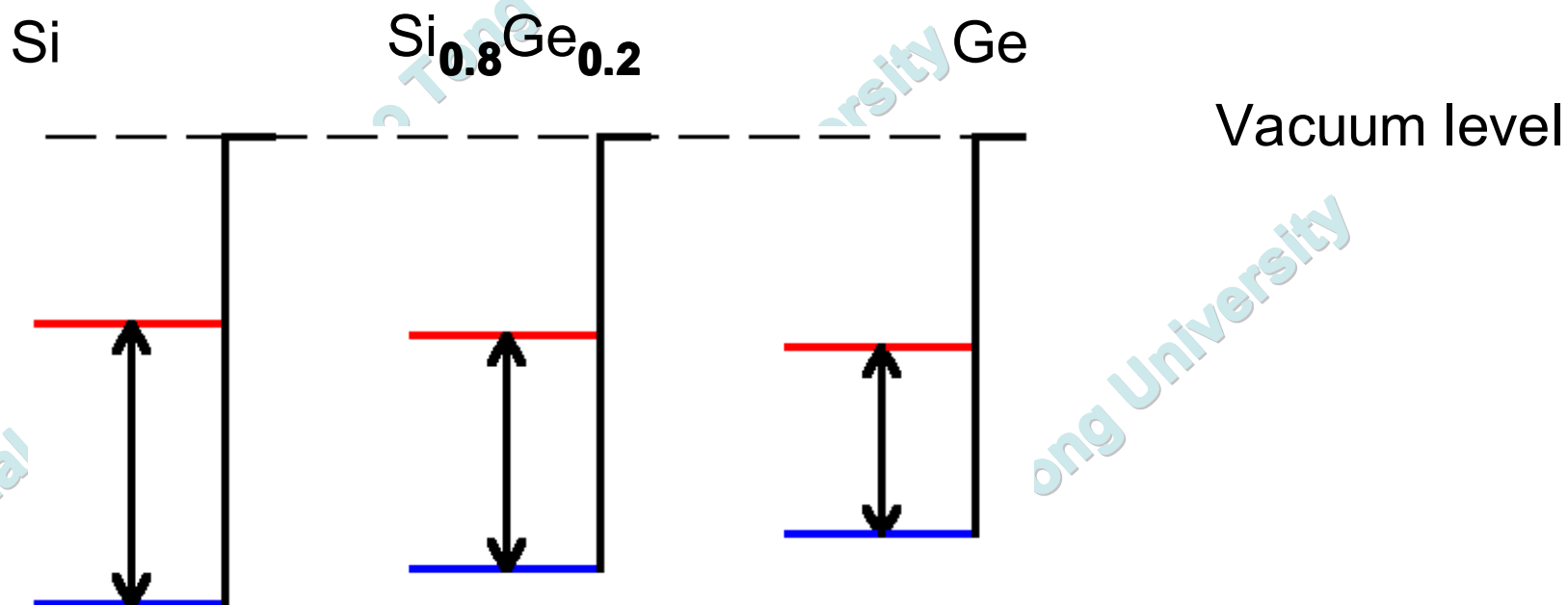


Si-Ge HBT's for BiCMOS





Bandgaps and alignments

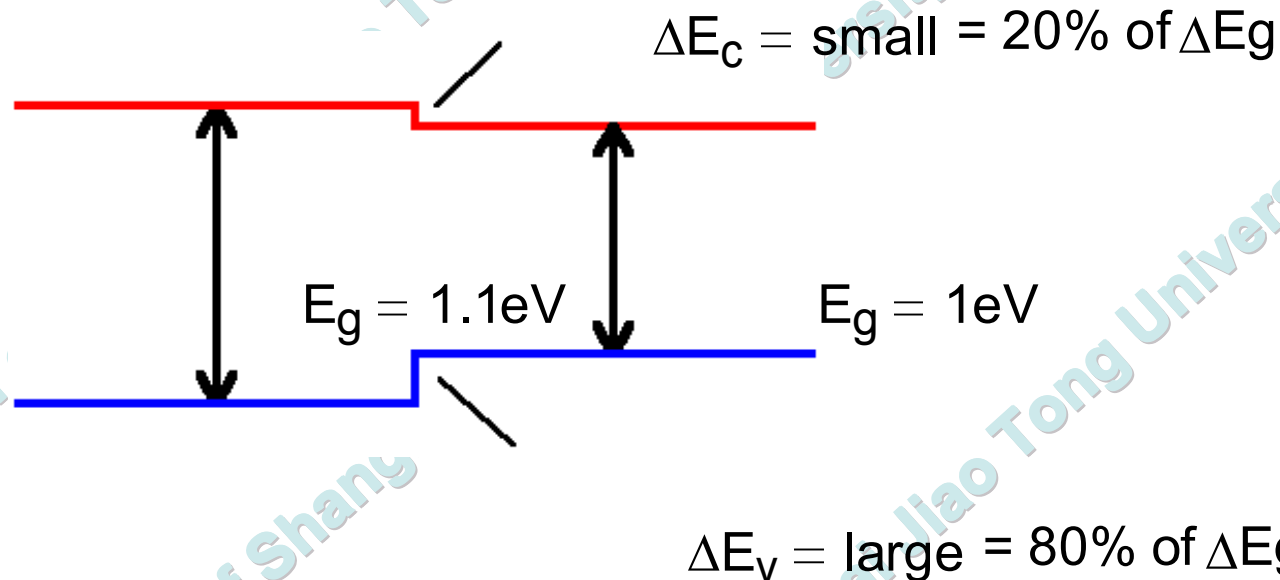




Si-Ge Heterostructure

Silicon:

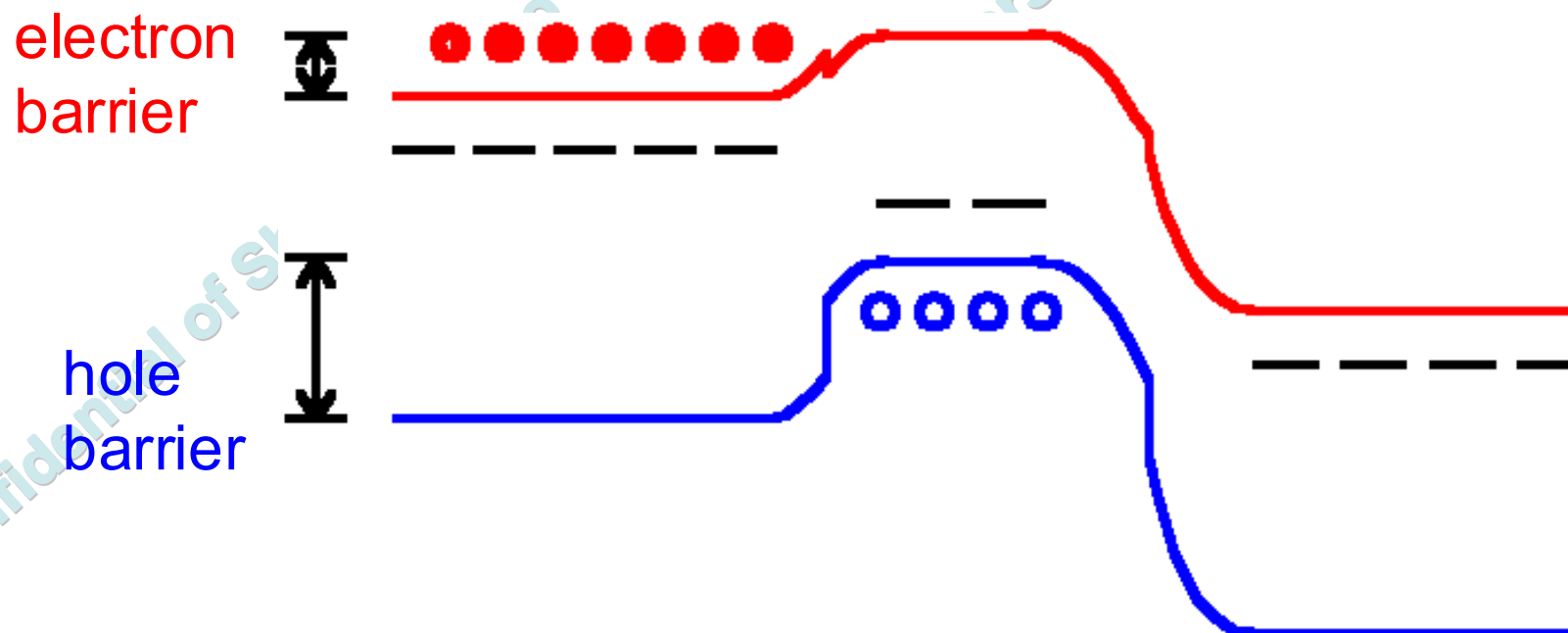
$\text{Si}_{0.8}\text{Ge}_{0.2}$:



 **Most of the bandgap difference shows up in the valence band**



Band Diagram for SiGe HBT



Hole barrier is higher by $\sim \Delta E_v \sim 0.1$ eV!!



For $\Delta E_V \sim 0.1$ eV, new exponential multiplier equals:

$$\sim e^{\frac{-\Delta E_V}{k \cdot T}} = e^{\frac{0.1}{0.0259}} = \frac{1}{50}$$

SiGe Heterojunction cuts backward hole injection by ~ 50 :

Use higher gain if needed

If more gain not needed, increase BASE DOPING by 50

- Retain gain of previous pure Si transistor
- Reduce "base resistance"

=> more efficient operation

=> FASTER operation (reduced R-C charging time)



Si-Ge HBT's

$$\beta_{dc} = D_B L_E N_E / D_E W N_B$$

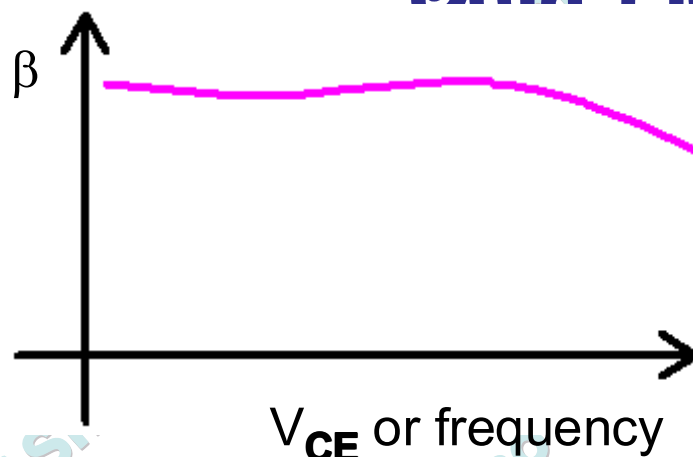
$$\beta_{dc} = D_B L_E (n_i^2 / N_B) / D_E W (n_i^2 / N_E)$$

$$\beta_{dc}^{HBT} = \beta_{dc} (n_{Si_i}^2 / (n_{Ge_i})^2)$$

$$= \beta_{dc} e^{(E_{Ge_i} - E_{Si_i}) / 2kT}$$



Gain Plots



On frequency versions can plot either:

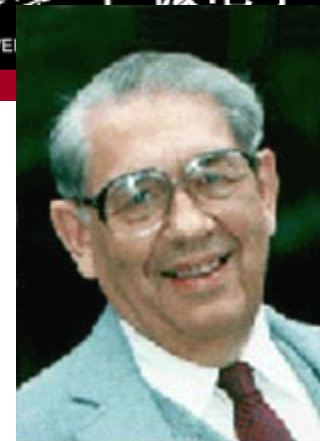
Power gain $\Rightarrow$ rolls downward at frequency = " $f_{\max}$ "

Current gain $\Rightarrow$ rolls downward at frequency = " f_t "

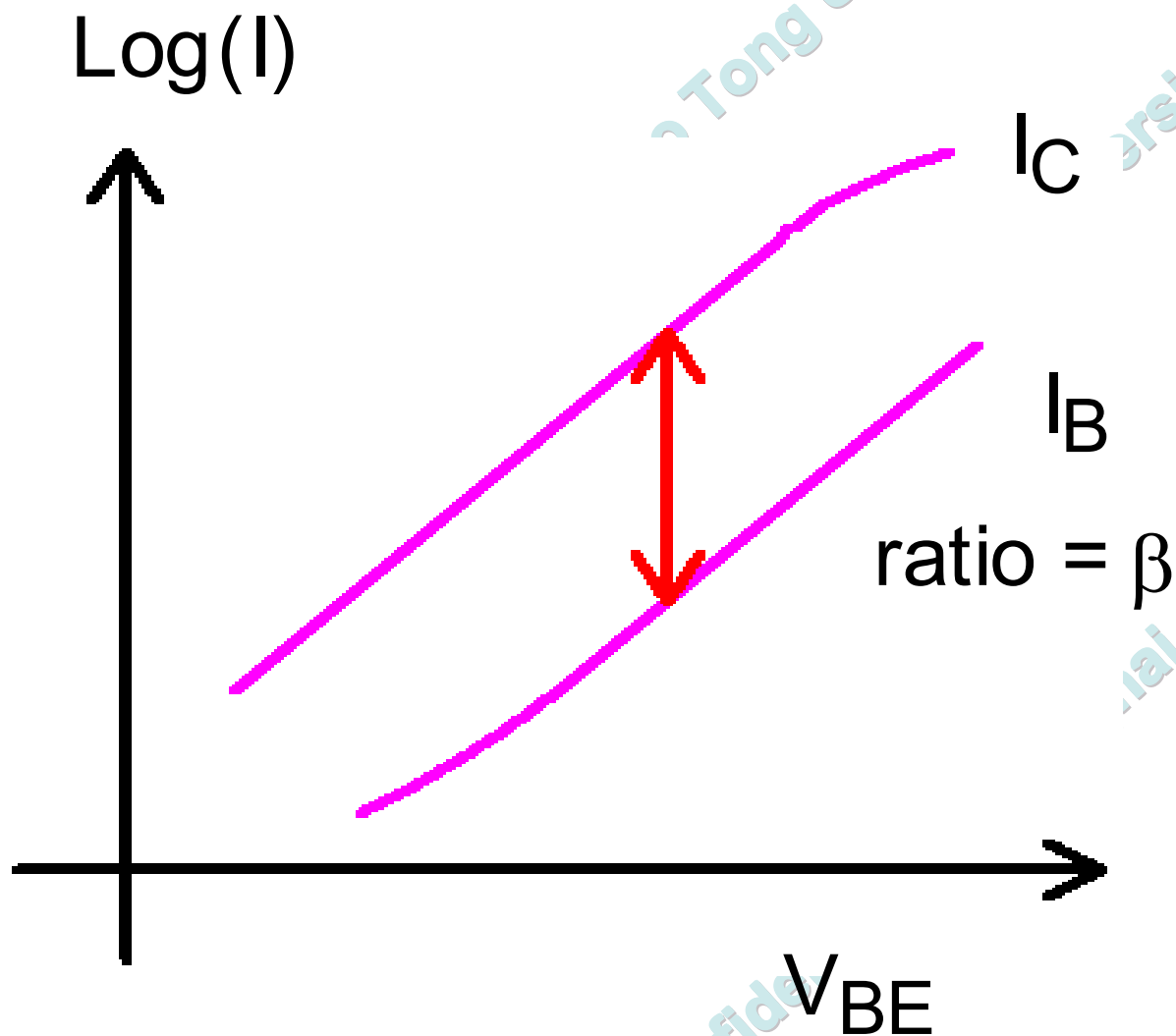
(Have seen designers ~ come to blows over which more important!)



Gummel Plot

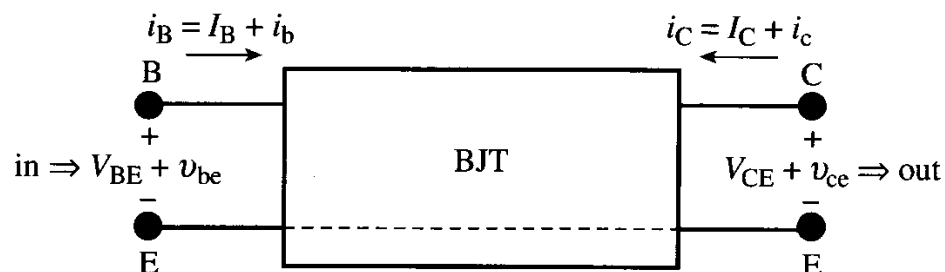


Hermann-Gummel

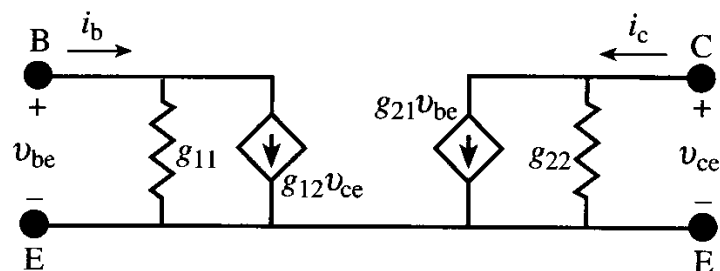




Assume the transistor can follow AC voltages and currents quasistatically (frequency not too high). Also neglect other



(a)



(b)

Common Emitter equivalent circuit model



BJT Small Signal Response

$$I_B = I_B(V_{BE}, V_{CE})$$

$$I_B(V_{BE} + V_{be}, V_{CE} + V_{ce}) = I_B(V_{BE}, V_{CE}) + \left. \frac{\partial I_B}{\partial V_{BE}} \right|_{V_{CE}} V_{be} + \left. \frac{\partial I_B}{\partial V_{CE}} \right|_{V_{BE}} V_{ce}$$

$$I_C = I_C(V_{BE}, V_{CE})$$

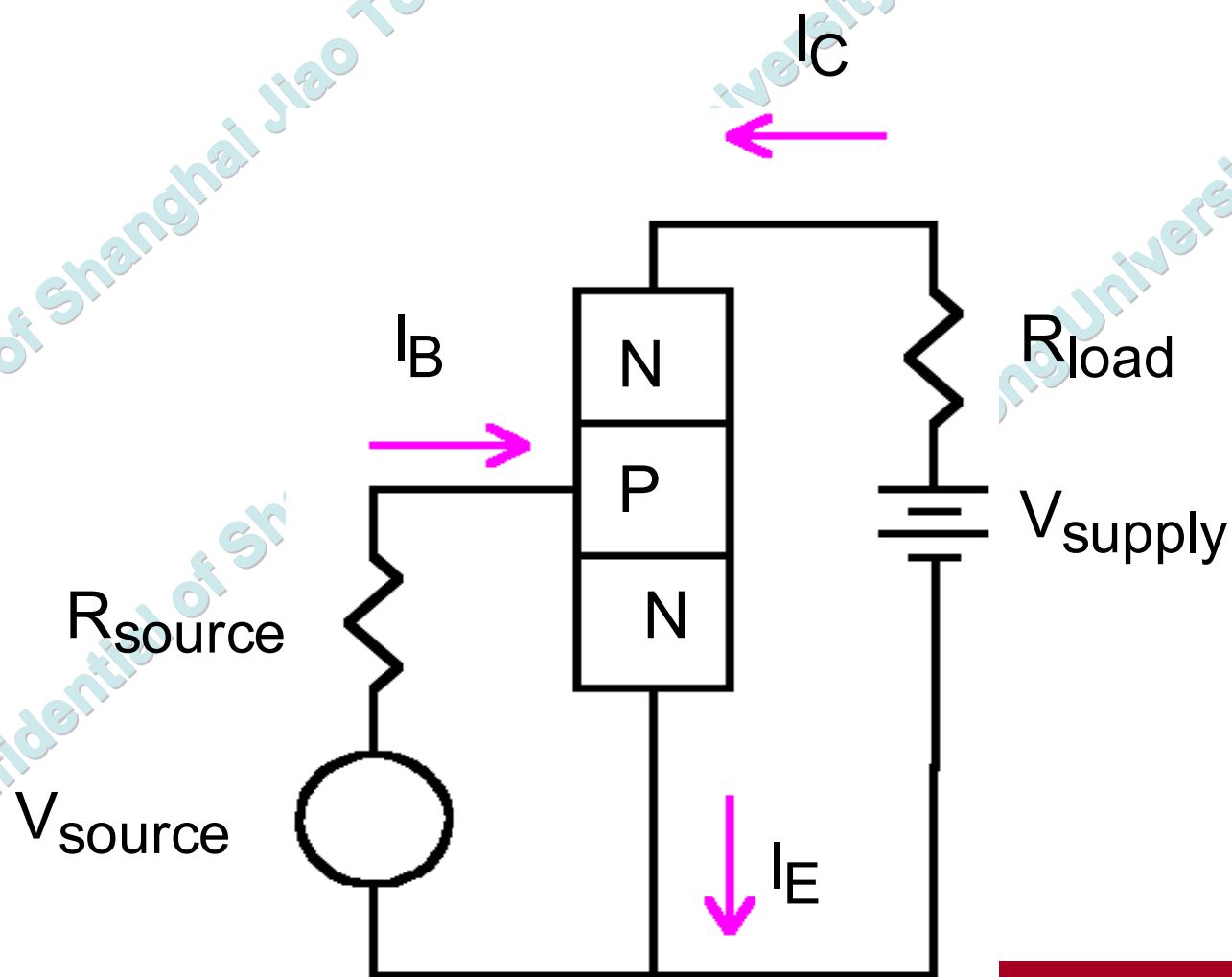
$$I_C(V_{BE} + V_{be}, V_{CE} + V_{ce}) = I_C(V_{BE}, V_{CE}) + \left. \frac{\partial I_C}{\partial V_{BE}} \right|_{V_{CE}} V_{be} + \left. \frac{\partial I_C}{\partial V_{CE}} \right|_{V_{BE}} V_{ce}$$

$$i_b = g_{11}V_{be} + g_{12}V_{ce}$$

$$i_c = g_{21}V_{be} + g_{22}V_{ce}$$

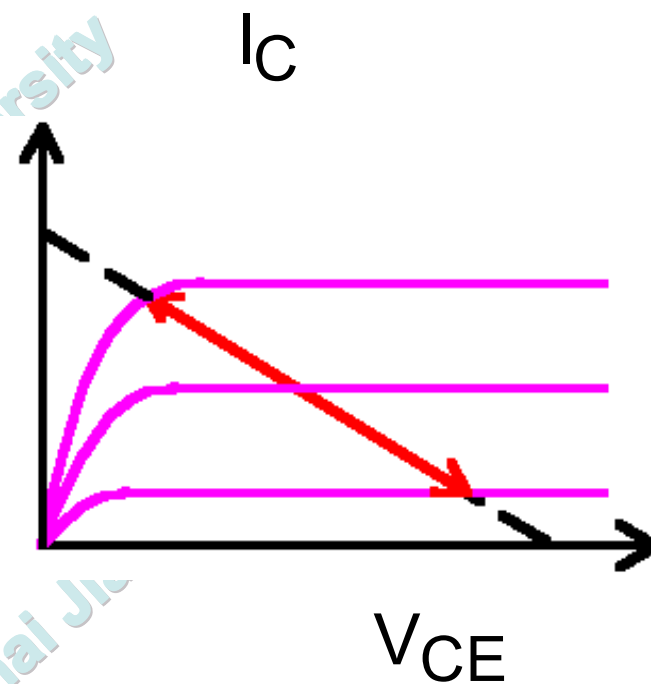
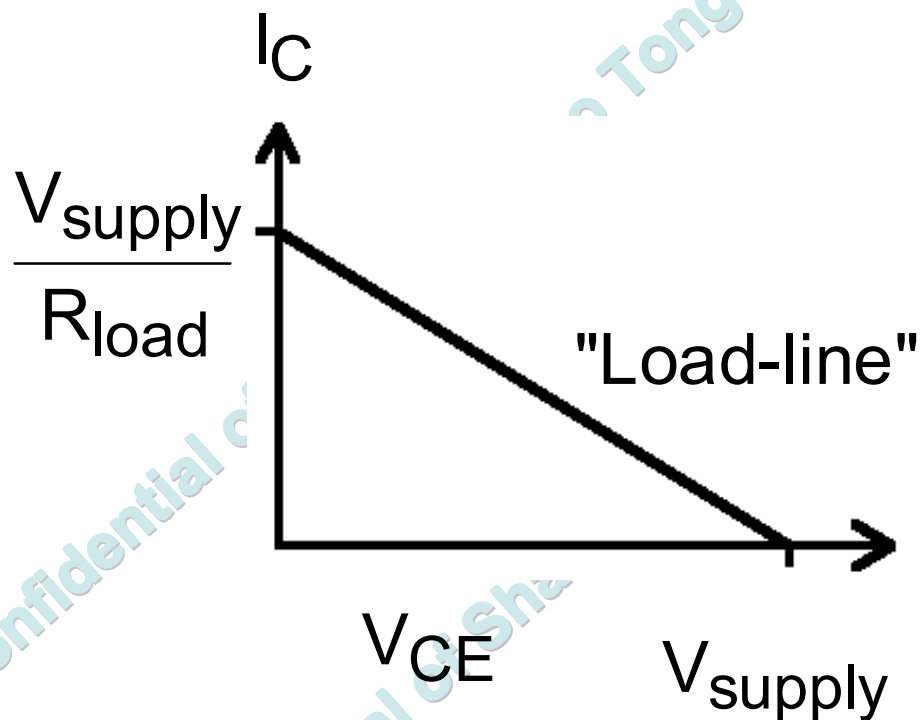


As with diodes, switching often limited by external circuit:





Right Circuit Loop:



Transistor is constrained by load-line:

