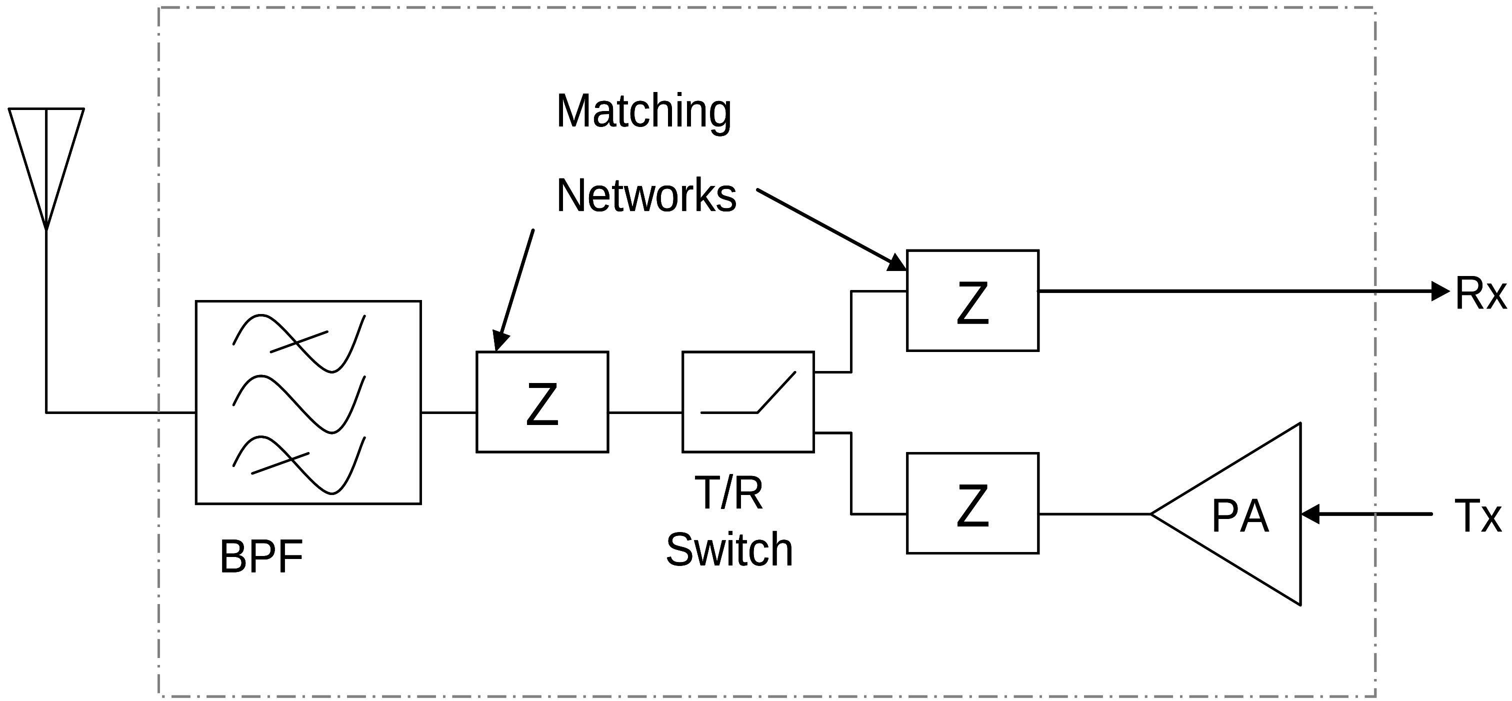
Introduction to CMOS RF Integrated Circuits Design

VII. Power Amplifiers

Outline

- Functionality
- Figures of Merit
- PA Design
  - Classical Design (Class A, B, C)
  - High-Efficiency Design (Class E, F)
- Matching Network
- Linearity
- T/R Switches

PAs and TRs Switching in Transceiver



Functionality of PAs

•To Amplify and Deliver Required Signal Power to Antenna at Frequency of Interest
•To Achieve Desired Output Power with Maximum Power Efficiency
•To Provide Output Impedance Matching to Antenna
•To Have Clean Spectrum Not to Affect Receivers

Figures of Merit of PAs

- Frequency
- Output Power
- Power Efficiency
- Linearity (P-1dB, IIP3, ACPR)
- Conversion Gain
- Spur

Output Power

$$P_o = \frac{v_{o,rms}^{2}}{R_L} = \frac{v_{o,amp}^{2}}{2R_L} = \frac{v_{o,p-p}^{2}}{8R_L}$$

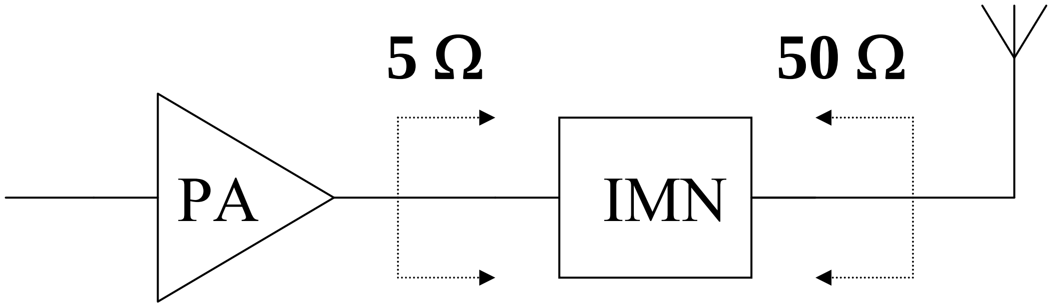
- For a Load of 50 Ohm, Need an Output Amplitude of 10 V to Achieve an Output Power of 1W!
- For a Low Supply, Need Small Load for Large Output Power, i.e. A 3.3-V Output Amplitude Can Only Deliver 1W to a Load of 5 Ohm!

Output Power

•Need an Output Impedance Matching to Convert 50 Ω to a Smaller Load!

•As Supply and Load Decrease, PA Would Need to Deliver Much Larger Current

•Loss Due to Parasitic (R, L) Becomes Significant => Low Efficiency!



Power Gain and Efficiency

$$A_P = \frac{P_o}{P_{in}}$$

$$\eta = \frac{P_o}{P_{DC}}$$

$$PAE = \frac{P_o - P_{in}}{P_{DC}}$$

•With a High Power Gain AP, Drain Efficiency η is Approximately the Same as Power-Added Efficiency PAE

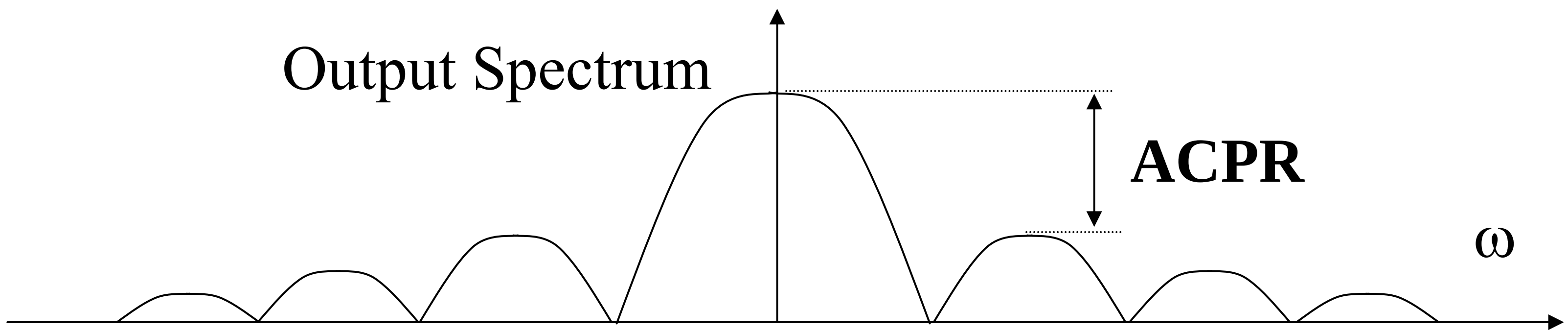
Linearity

- 1-dB Compression Point
- Intermodulation Intercept Point IIP3
- Conventional Definition and Measurement Not Sufficient Because Most PAs Operate Near 1-dB Compression Point for Maximum Efficiency => Higher-Order Distortion Becomes Significant and Needs to Be Included => Adjacent-Channel Power Rejection ACPR

Adjacent-Channel Power Rejection (ACPR)

•A Modulated Signal is Applied to Include High-Order Distortion

•ACPR is Defined and Measured as the Power of the Adjacent Channel Relative to the Carrier

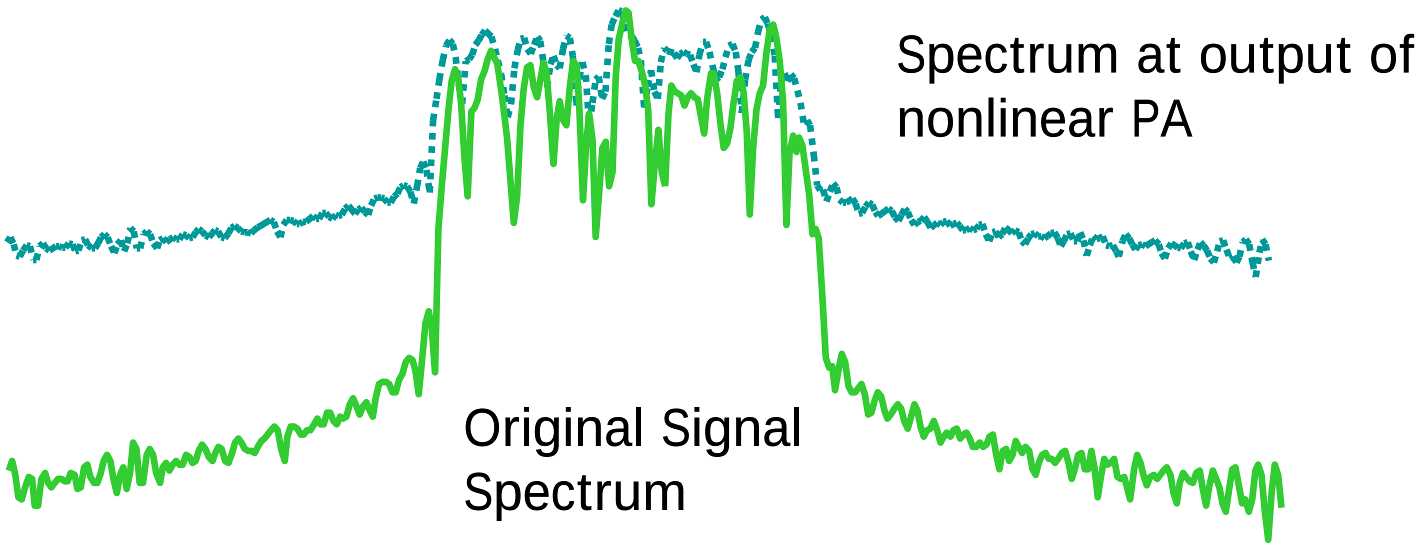


Typical Figures of Merit

Output Power	~ 0 – 35 dBm
Efficiency	~ 30 – 60 %
Gain	> 20 dB
Linearity, IMD	- 30 dBc
Linearity, ACPR	- 25 dBc
Spurs	< - 50 dBc
Supply Voltage	~ 1.8 V
Current	> 300 mA

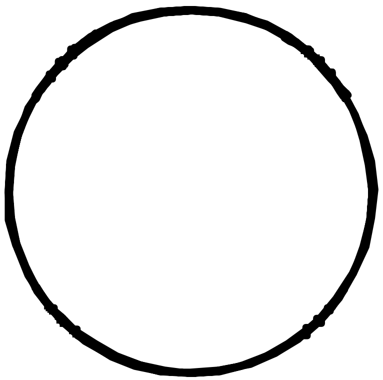
Linear Power Amplifiers

•Linear Relationship between Input and Output Signals
•Critical for Applications with Non-Constant Envelope Modulation Scheme
•Classical Linear PAs Include Class-A, Class-B, and Class C
•Classification is Made Based on Conduction Angle, Defined as the Fraction of Period when Active Device is On



Non-Linear Power Amplifiers

Constant envelop modulation



GMSK
FSK

Nonlinear PA
High Efficiency

Nonconstant envelop modulation

BPSK
QPSK
QAM

Linear PA
Low Efficiency

Conduction Angle

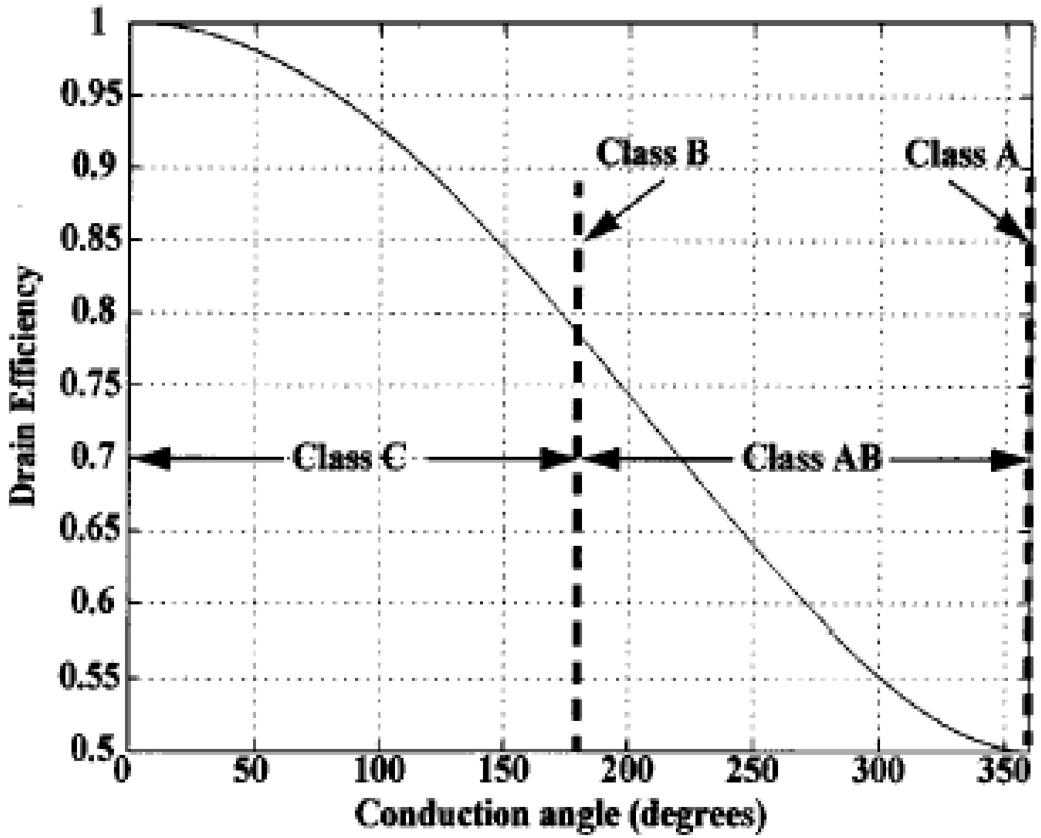
$$P_o = \frac{\theta - \sin\theta}{1 - \cos(\theta/2)}$$

$$\eta = \frac{P_o}{P_{DC}} = \frac{1}{4}\frac{\theta - \sin\theta}{\sin(\theta/2) - (\theta/2)\cos(\theta/2)}$$

Class	A	B	C
θ	360	180	0
η	50%	78%	100%

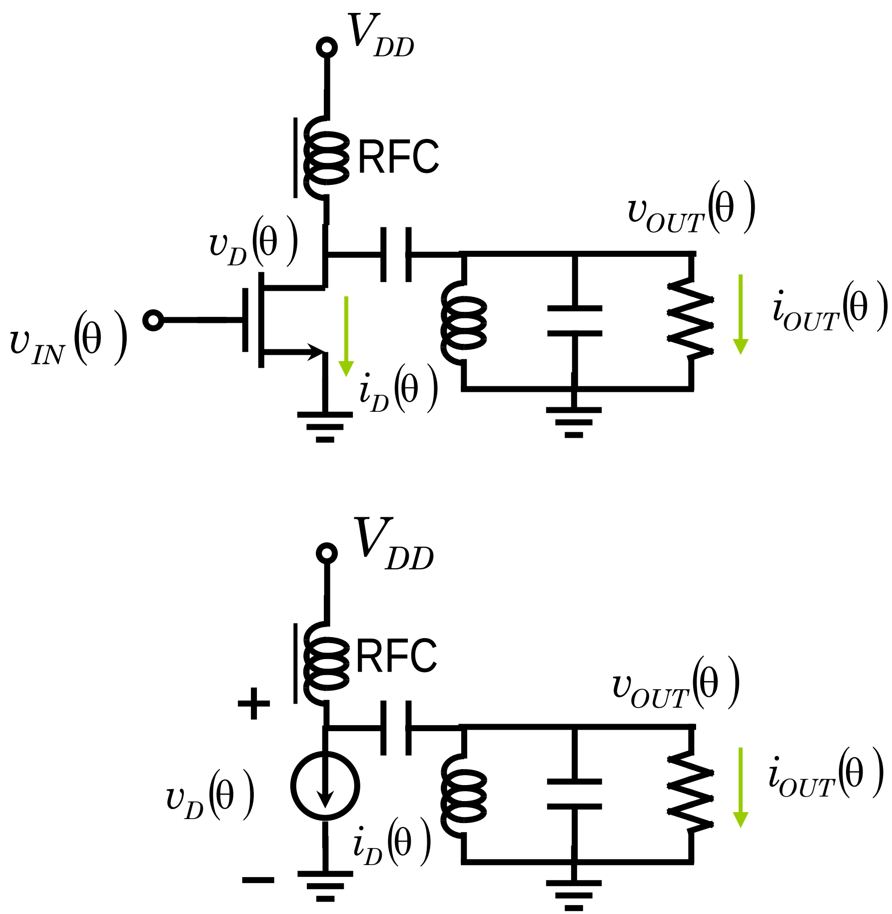
REF: H. Kraus, et al, *Solid State Radio Engineering*, Wiley, 1980

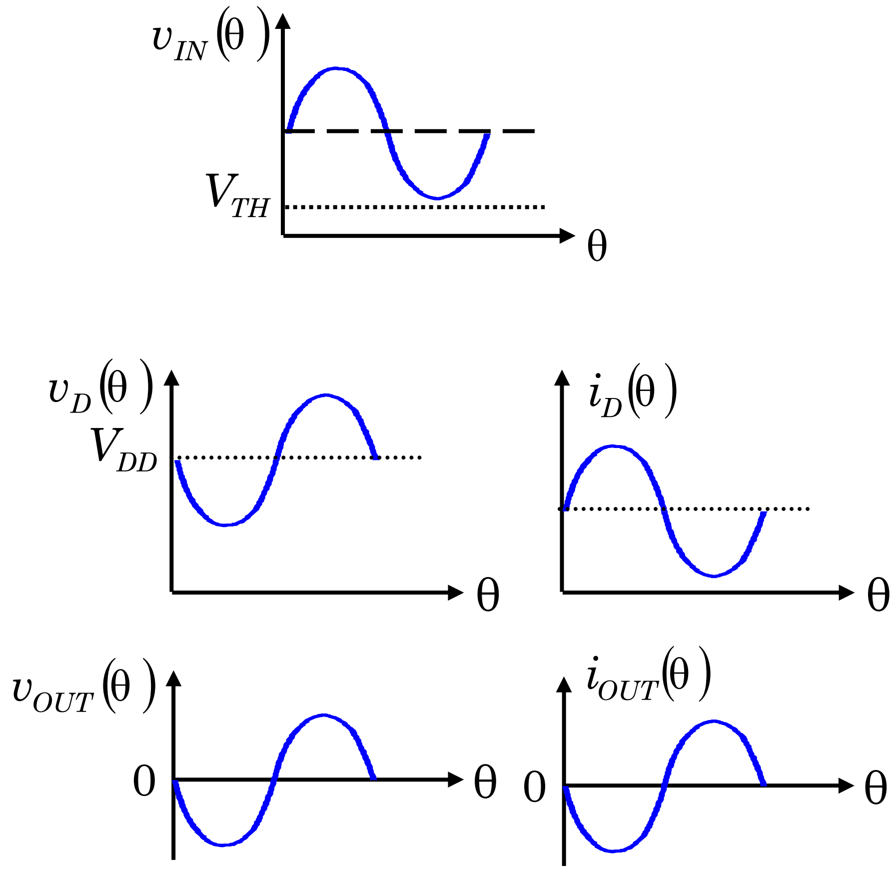
Conduction Angle



REF: H. Kraus, et al, *Solid State Radio Engineering*, Wiley, 1980

Class-A Power Amplifiers





Class-A Power Amplifiers

- Single Transistor as Amplifier to Minimize Loss and Maximize Efficiency
- Transistor Always Conducts => Conduction Angle is 360 Degrees
- Highest Linearity
- Lowest Efficiency

Class-A Power Amplifiers

•RF Choke LC Provides Constant Bias Current Source While Doubling Output Voltage and Efficiency (as Compared to Resistive Load)
•Capacitor Cb Blocks DC Current from Flowing to the Output => No DC Power Consumption for the Load
•Resonant Tank Filters Harmonics Due to Non-Linearity to Obtain Single Tone at Output

Class-A Power Amplifiers

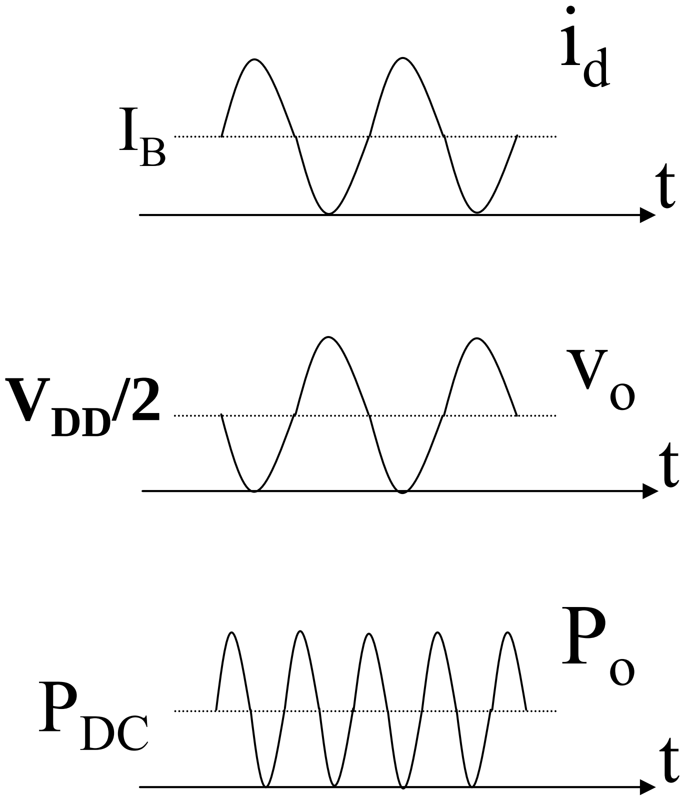
•For Resistive Load, Maximum Output Voltage is Limited to V_{DD}

•For Inductive Load, Maximum Output Voltage is Increased to $2V_{DD}$

For Same Loading and Same Supply, Output Power is Increased By 4 Times and Efficiency is Increased By 2 Times

For Same Loading and Same Output Power, Supply Can Be Reduced By 2 Times

Class-A PA with Resistive Load

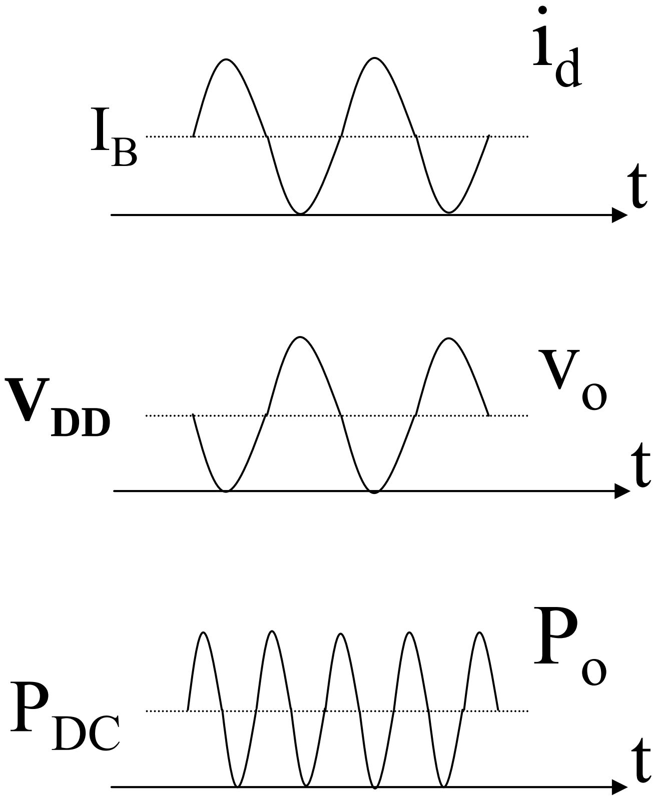


$$P_{o,max} = \frac{V_{o,max} I_{o,max}}{2} = \frac{V_{DD} I_B}{4}$$

$$P_{DC} = V_{DD} I_{D,ave} = V_{DD} I_B$$

$$\eta_{max} = \frac{P_{o,max}}{P_{DC}} = 25\%$$

Class-A PA with Inductive Load



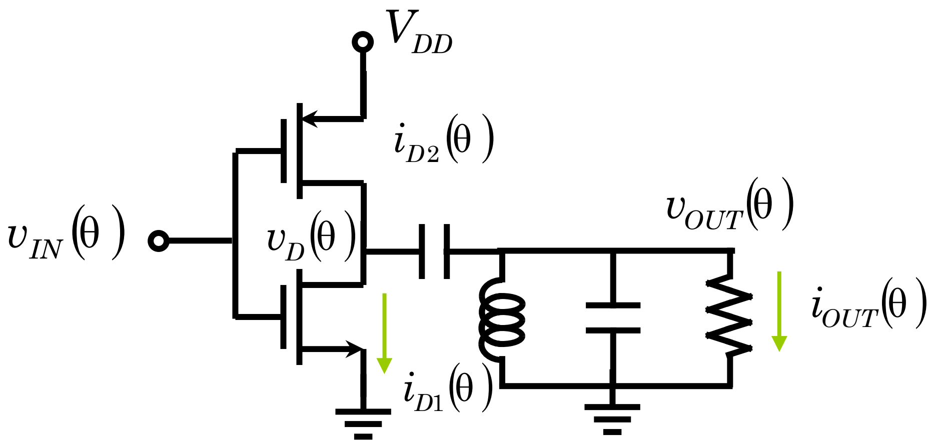
$$P_{o,\max} = \frac{V_{o,\max} I_{o,\max}}{2}$$

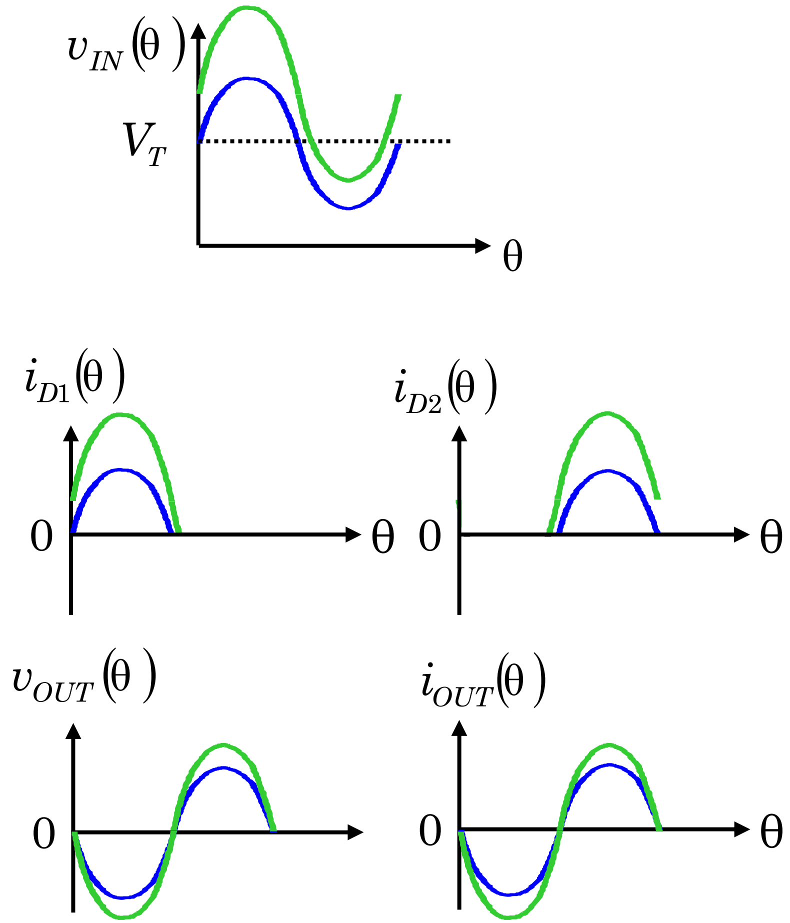
$$= \frac{V_{DD} I_B}{2}$$

$$P_{DC} = V_{DD} I_{D,ave} = V_{DD} I_B$$

$$\eta_{\max} = \frac{P_{o,\max}}{P_{DC}} = 50\%$$

Class-B Power Amplifiers





$$P_{RFout} = \frac{V_{om}^{2}}{2R} \le \frac{V_{DD}^{2}}{2R}$$

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} I_D|\sin\theta|d\theta = \frac{2I_D}{\pi} = \frac{2}{\pi}\frac{V_{om}}{R}$$

$$\eta_{Drain} = \frac{P_{RFout}}{P_{DC}} = \frac{V_{om}^{2}/2R}{\frac{2}{\pi}\frac{V_{om}}{R}V_{DD}} = \frac{\pi}{4}\frac{V_{om}}{V_{DD}} \le \frac{\pi}{4} \approx 0.785$$

Class-B Power Amplifiers

- Two Transistors as Push-Pull Amplifier
- Transistors Conduct Only HALF CYCLE => Conduction Angle is 180 Degrees
- Higher Efficiency Compared to Class-A
- Compromised Linearity
- Due to Speed Limitation of PMOS, Two NMOS Can Be Used In Parallel with Their Currents Combined By a Transformer

Class-B Power Amplifier

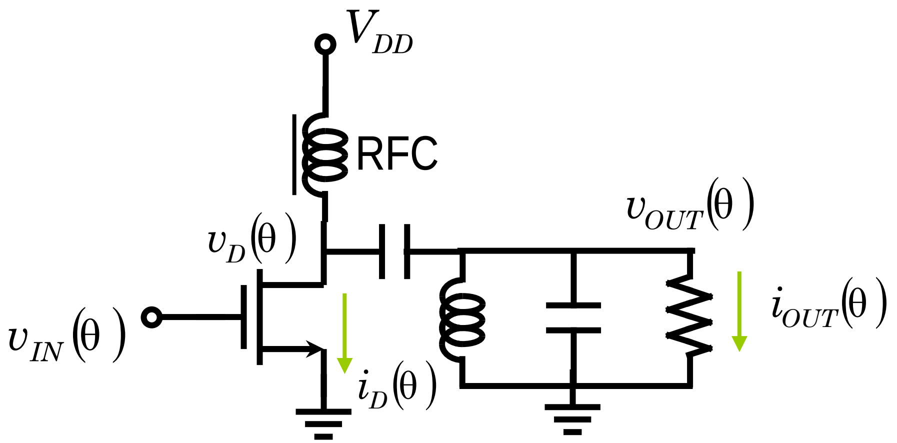
$$P_{o,\max} = \frac{V_{o,\max} I_{o,\max}}{2} = \frac{V_{DD}^{2}}{4R_L}$$

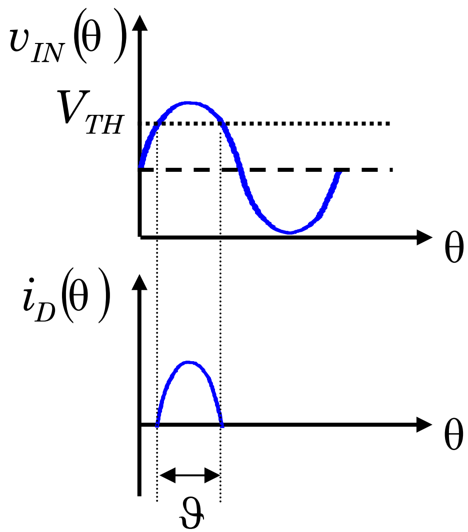
$$I_{D,ave} = \frac{V_{DD}}{\pi R_L}$$

$$P_{DC} = V_{DD} I_{D,ave} = \frac{V_{DD}^{2}}{\pi R_L}$$

$$\eta_{\max} = \frac{P_{o,\max}}{P_{DC}} = \frac{\pi}{4} = 78\,\%$$

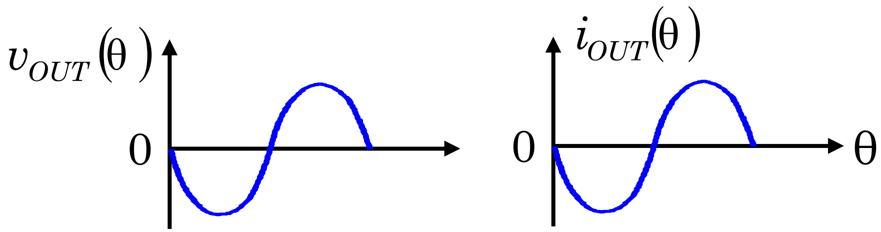
Class-C Power Amplifiers





$$P_{RFout} \propto \frac{\vartheta - \sin\vartheta}{1 - \cos(\vartheta/2)}$$

$$\eta_{Drain} = \frac{P_{RFout}}{P_{DC}} = \frac{1}{4}\frac{\vartheta - \sin\vartheta}{\sin(\vartheta/2) - \vartheta/2\cos(\vartheta/2)}$$



Class-C Power Amplifiers

- Transistor Conducts Much Less Than Half of Cycle => Conduction Angle is Close to Zero Degree
- Higher Efficiency Compared to Class-A and Class-B
- Much Degraded Linearity
- Lower Output Power

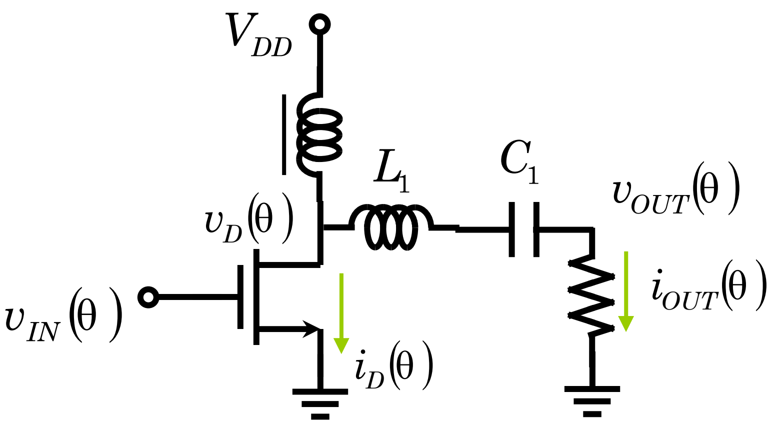
Non-Linear Power Amplifiers

- Operate Active Devices as Switches Instead of Amplifying Linear Devices
- Highly Non-Linear
- Highest Efficiency (~ 100%)
- Most Suitable for Applications with Constant-Envelope Modulation
- For Linear Applications, Need Linearization Techniques
- Includes Class-E, Class-F

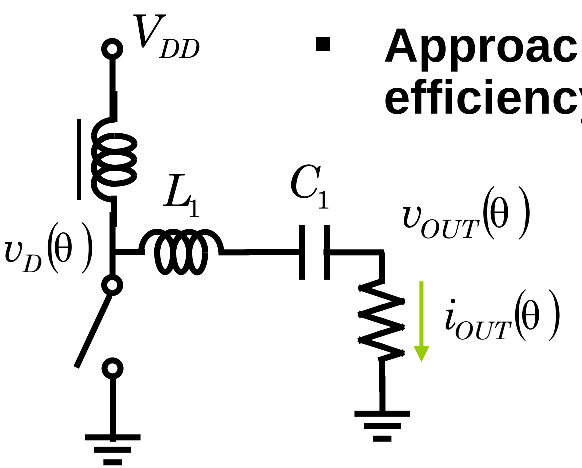
Non-Linear Power Amplifiers

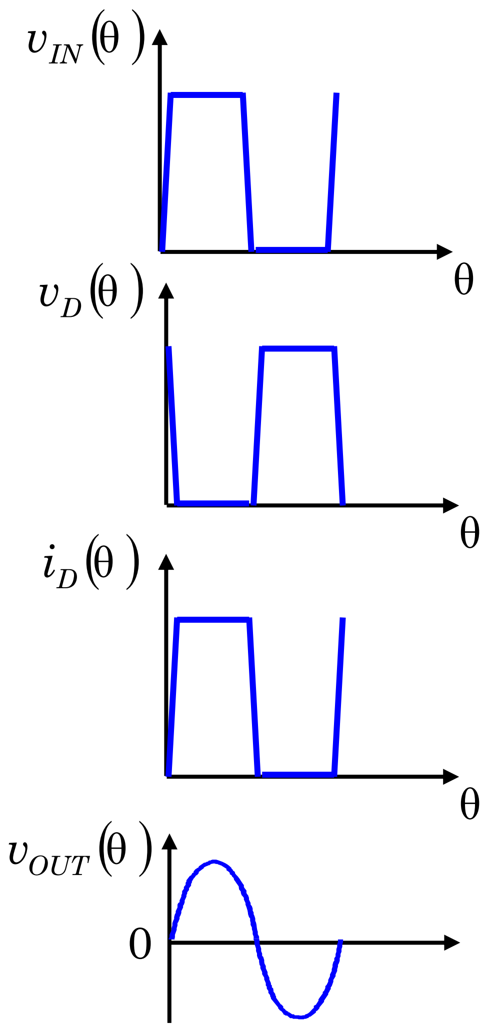
- In Practice, Efficiency is Limited to ~ 60% Due to:
  - High Speed => Not Too Large Device Size => Finite Turn-On Resistance of the Switch
  - Finite Turn-On Transition Times
  - Low-Q Inductors => Off-Chip Inductors or Bond Wires
- For High Output Power, Device Stress is Critical

Class-E Power Amplifiers



- **Switch mode**
- **Approaching 100% efficiency**

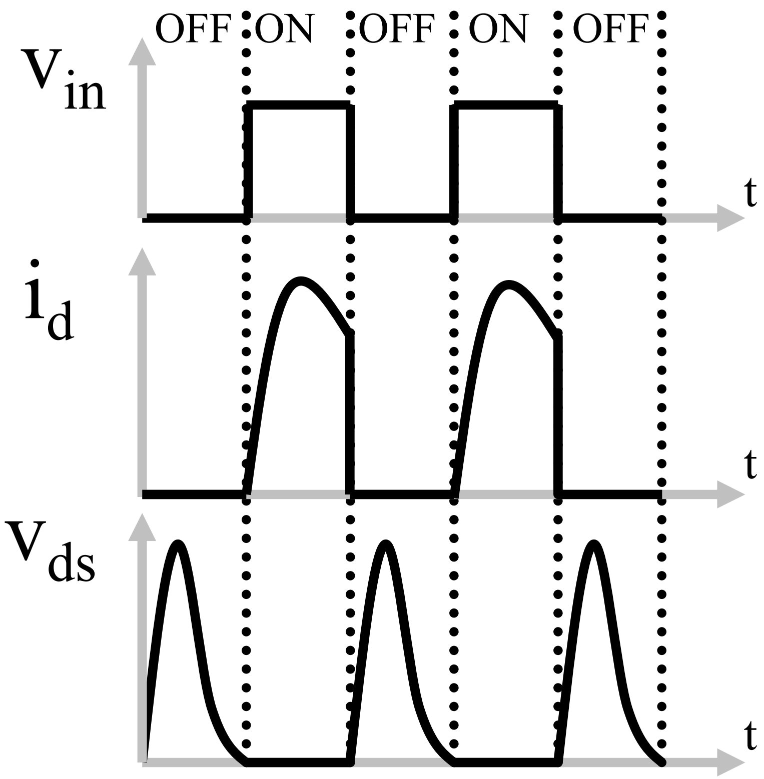




Class-E Power Amplifiers

- Operate Active Device as Switch To Minimize Power Loss and Maximize Efficiency (~ 100%) :
  - Small Transition Times Between ON and OFF
  - Small Voltage when Conducting Current
  - Small Current when Sustaining Large Voltage
  - Change of Voltage with Time is Close to Zero when Starting Conducting
- Parasitic Capacitance of Device Can Be Conveniently Absorbed in Cd

Class-E Power Amplifiers



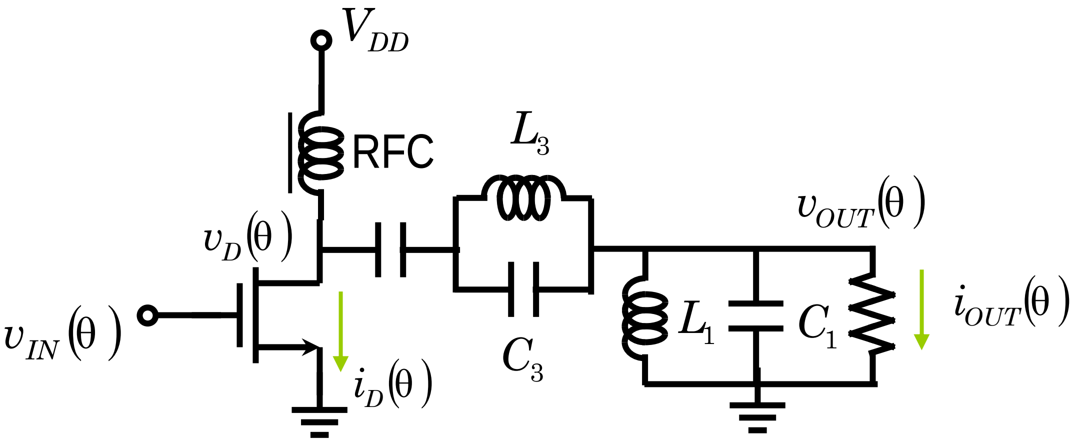
$$L_r = \frac{\pi V_{DD}^2 (\pi^2 - 4)}{2\omega(\pi^2 + 4)}$$

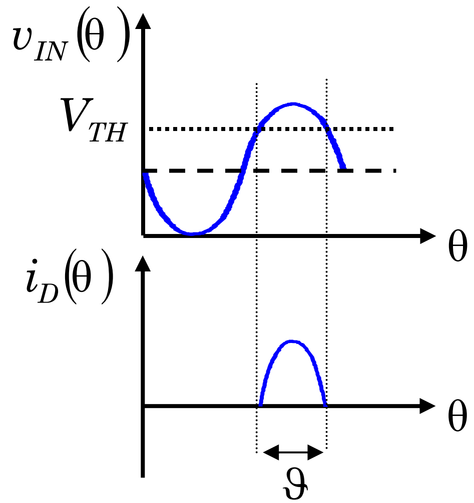
$$C_d = \frac{P_o}{\pi \omega V_{DD}^2}$$

$$R_{opt} = 0.58 \frac{V_{DD}^2}{P_o}$$

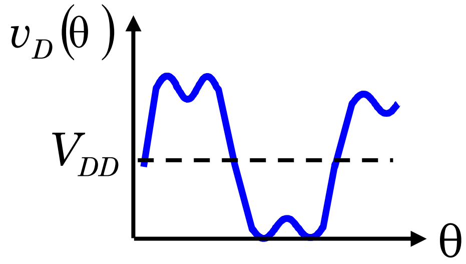
.

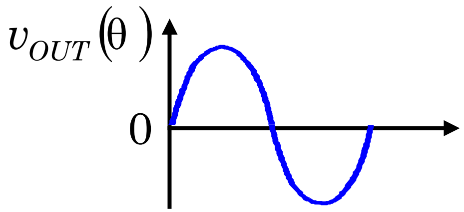
Class-F Power Amplifiers





- L_3C_3 tuned to the 2nd or 3rd harmonics
- Peak efficiency
  - 88% for 3rd harmonics peaking
  - 85% for for 2nd harmonics peaking.





Class-F Power Amplifiers

•Employ Harmonics to Simulate a Square Waveform to Minimize Transition Times and thus to Reduce Loss

•A Parallel Tank Lr3Cr3 is Included to Obtain a Third-Order Harmonic and to Add to the Fundamental to Approximate a Square Wave

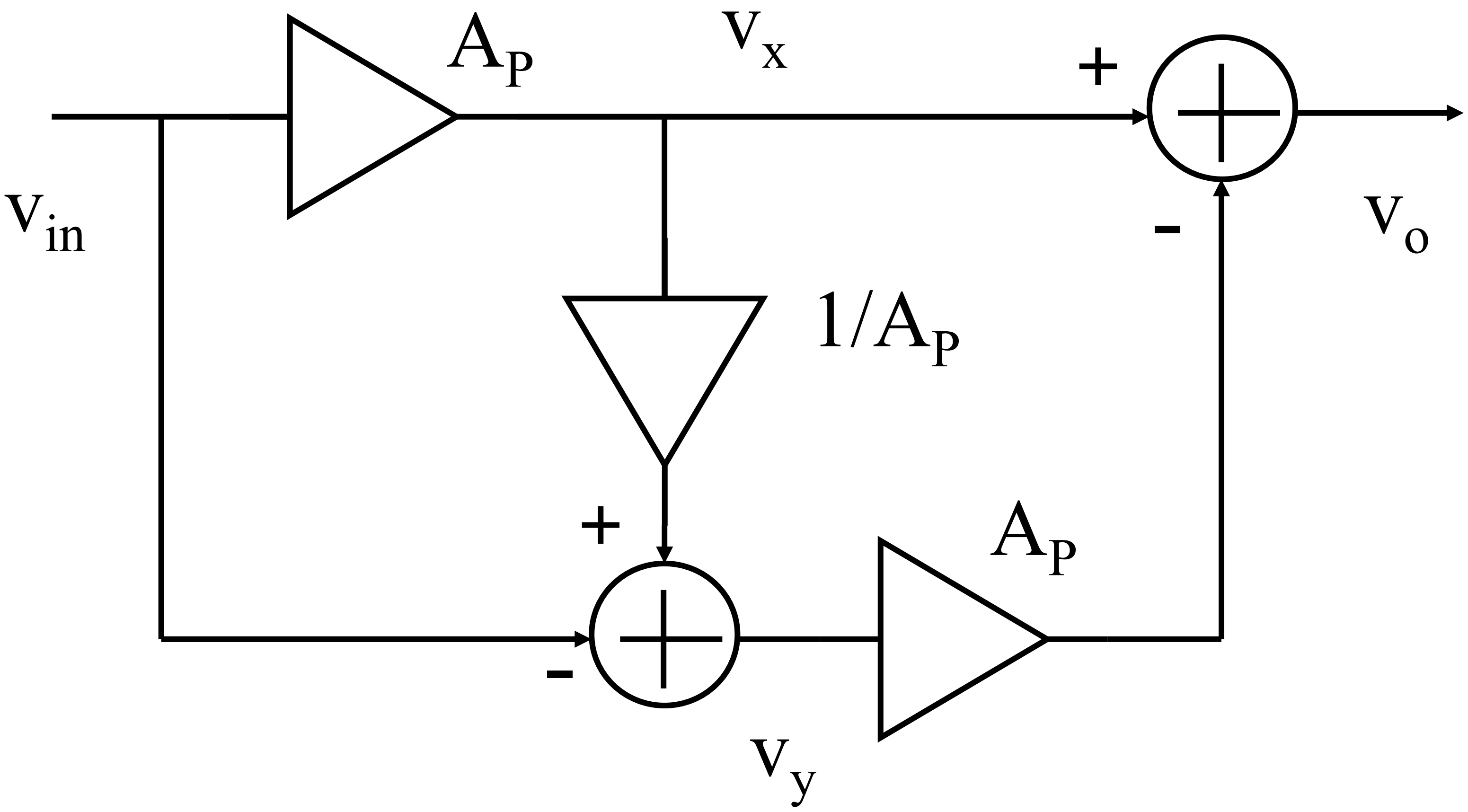
Challenges for CMOS PAs

- Trade-Off Among All Parameters
  - Speed
  - Device Size
  - Current and Output Power
  - Supply Voltage
  - Loss and Efficiency
  - Device Stress
- Low-Q On-Chip Inductors => Off-Chip Inductors or Bond Wires for Inductors in Resonant Tanks and Matching Network

Linearization Techniques

•Critical for Both High Efficiency and High Linearity
•Use Non-Linear Power Amplifiers (Class E and/or F) for High Efficiency
•Use Linearization Techniques to Improve Linearity:
- •Feed-Forward
- •Envelope Elimination and Restoration

Feed-Forward Techniques



Feed-Forward Techniques

$$v_o = v_x - A_v v_y$$

$$v_x = A_v v_{in} + \Delta v$$

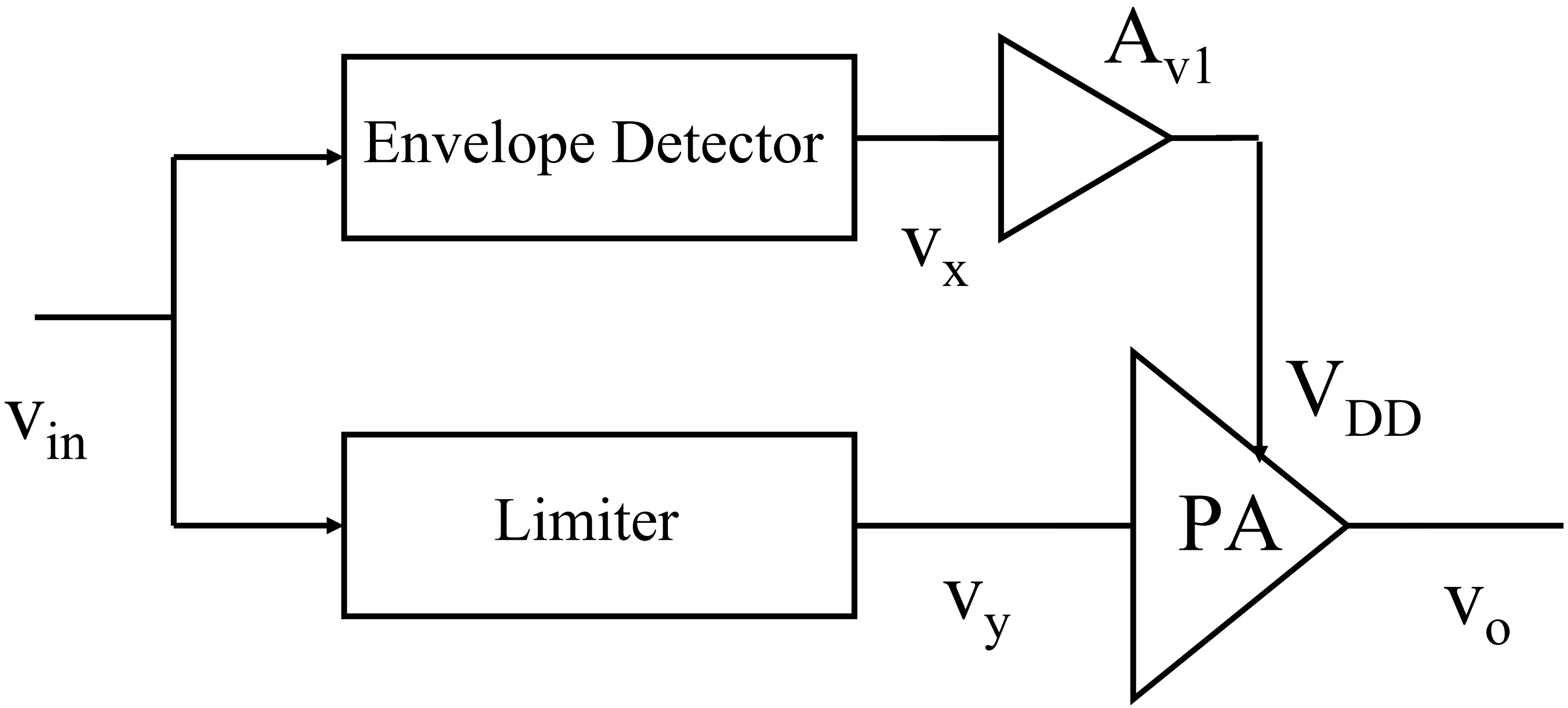
$$v_y = \frac{A_v v_{in} + \Delta v}{A_v} - v_{in} = \frac{\Delta v}{A_v}$$

$$\therefore v_o = v_x - A_v v_y = A_v v_{in}$$

Feed-Forward Techniques

- Open Loop Without Feedback => Unconditional Stability
- Limited Linearity Improvement Due to:
  - Gain Mismatches
  - Phase Mismatches
  - Errors of Subtractors
- Can Be Extended to Nested Feed-Forward Loops to Improve Linearity at A Cost of More Complexity

Envelope Elimination and Restoration (EER) Techniques



Envelope Elimination and Restoration (EER) Techniques

- Decompose Input Signal into An Envelope and a Phase-Modulated Signal, both of which are Amplified Separately and Recombined
- Constant-Envelope High-Frequency Phase-Modulated Component is Generated by "Eliminating" from Input's Envelope Using a Limiter and then Applied as Input to a High-Efficiency Switching PA

Envelope Elimination and Restoration (EER) Techniques

•Non-Constant Low-Frequency Envelope Can Be Extracted by an Envelope Detector, Amplified by a Switching Supply Voltage, and then "Recombined" with RF Phase-Modulated Component By Modulating the PA's Supply Voltage

•Achieve Linearization without Sacrificing Efficiency

Envelope Elimination and Restoration (EER) Techniques

•Operating Frequencies of the Two Paths are Quite Different
•Suffer from Phase and Gain Mismatches => Limited Linearity Improvement
•Power Consumption Can Be High => Power Efficiency Can Be Degraded