Introduction to CMOS RF Integrated Circuits Design

VI. Phase-Locked Loops

Outline

- Introduction
- Basic Feedback Loop Theory
- Circuit Implementation

What is a PLL?

•A PLL is a negative feedback system where an oscillator-generated signal is phase and frequency locked to a reference signal.

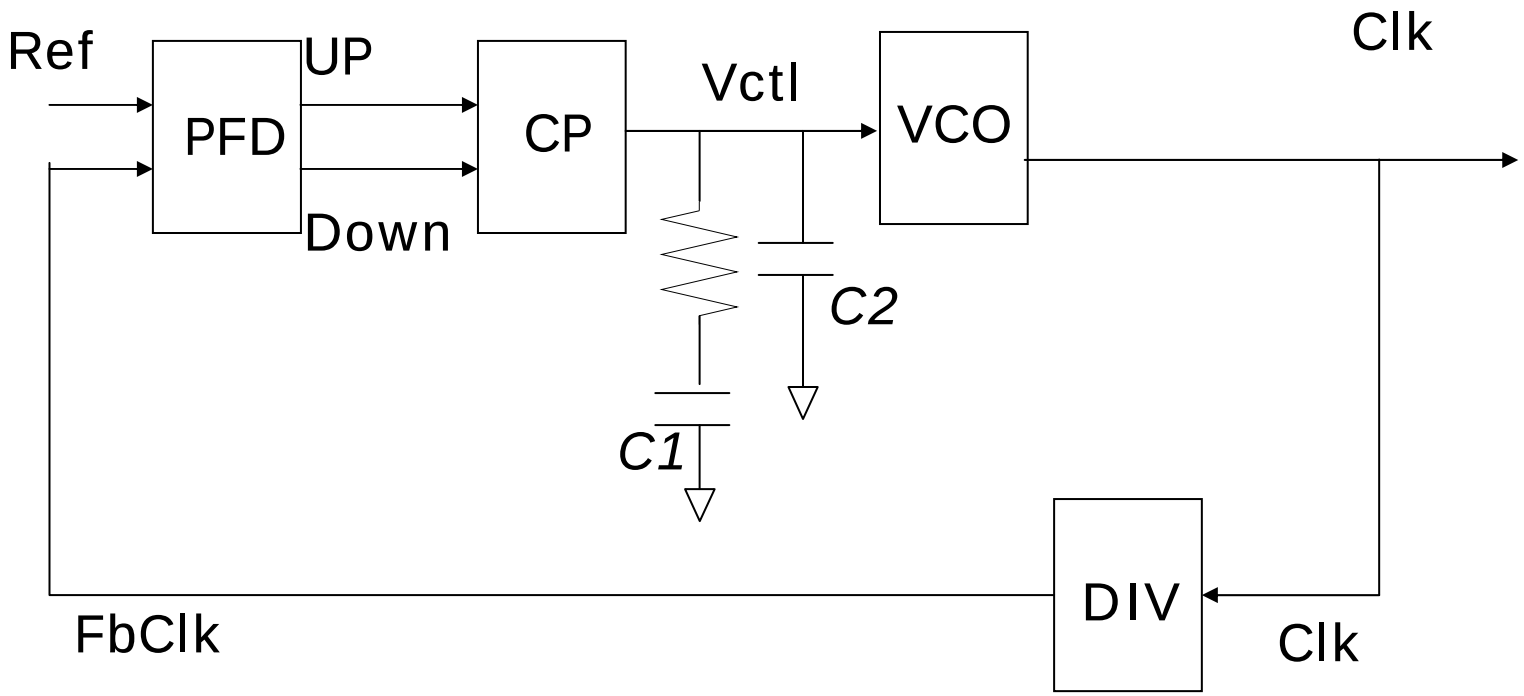
Can be used as:

•Frequency Synthesis (e.g. generating a 1 GHz clock from a 100 MHz reference)

•Skew Cancellation (e.g. phase-aligning an internal clock to the IO clock) (May use a DLL instead)

•Extracting a clock from a random data stream (e.g. serial-link receiver)

Charge-Pump PLL Block Diagram



Components in a Nutshell

•PFD: outputs digital pulse whose width is proportional to phase error
•CP: converts digital error pulse to analog error current
•LPF: integrates (and low-pass filters) error current to generate VCO control voltage
•VCO: low-swing oscillator with frequency proportional to control voltage
•DIV: divides VCO clock to generate FBCLK clock

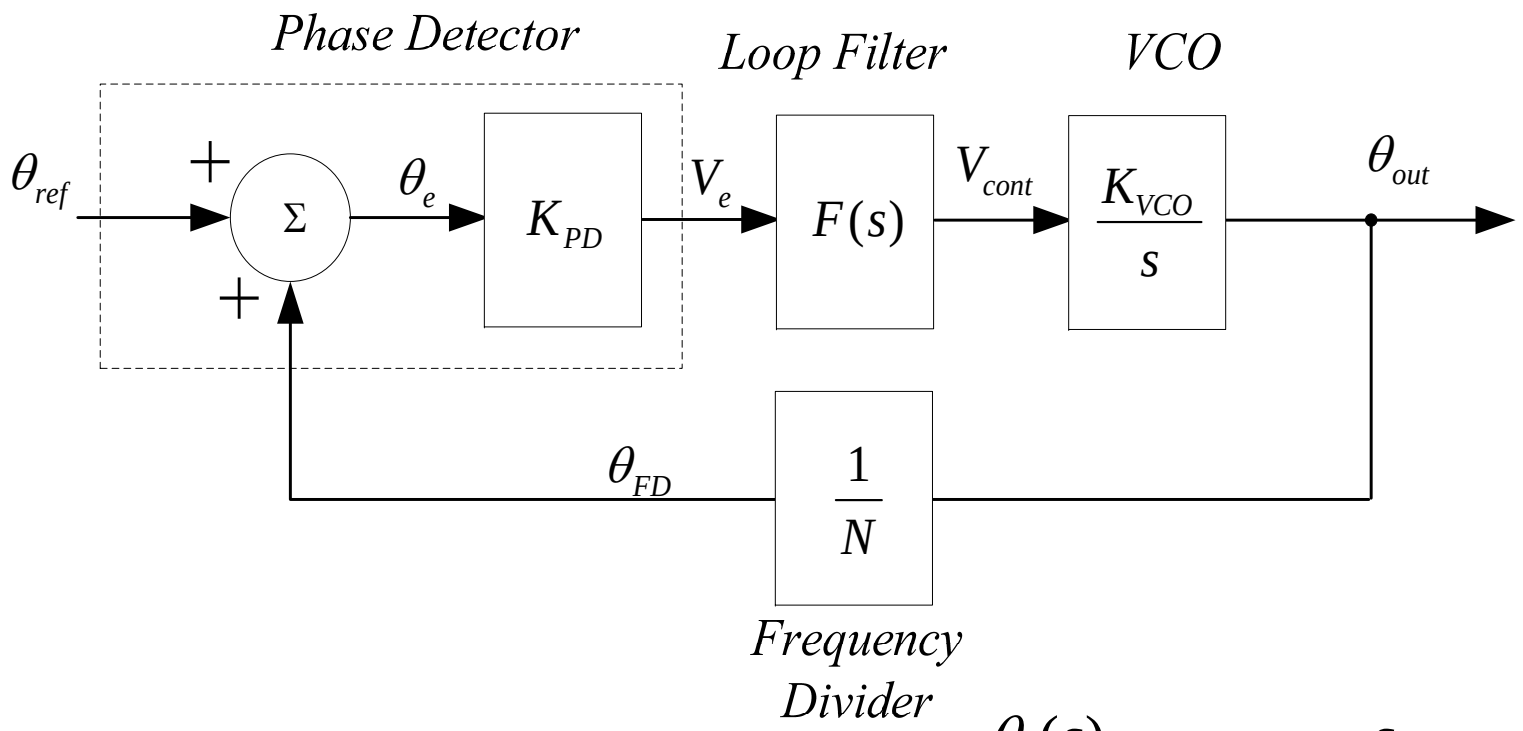
Is My PLL Stable?

•PLL is 2nd-order system similar to mass-spring-dashpot or RLC circuit.
•PLL may be stable or unstable depending on phase margin (or damping factor).
•Phase margin is determined from linear model of PLL in frequency-domain.
•Find phase margin/damping using MATLAB, loop equations, or simulations.
•Stability affects phase error, settling, jitter.

What Does PLL Bandwidth Mean?

- PLL acts as a low-pass filter with respect to the reference signal.
- Low-frequency reference modulation (e.g.spread-spectrum clocking) is passed to the VCO signal.
- High-frequency reference jitter is rejected.
- "Bandwidth" is the frequency at which the PLL begins to lose lock with the reference (-3dB).
- PLL acts as a high-pass filter wrt VCO noise.
- Bandwidth affects phase error, settling, jitter.

PLL Linear Model

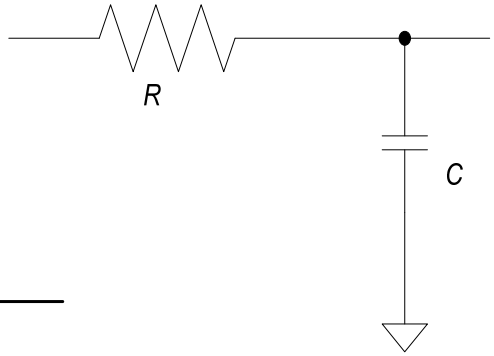


$$H(s) = \frac{\theta_{out}(s)}{\theta_{ref}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

$$\frac{\theta_e(s)}{\theta_{ref}(s)} = \frac{s}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

PLL Linear Model

$$F(s)=\frac{1}{(1+sRC)}$$



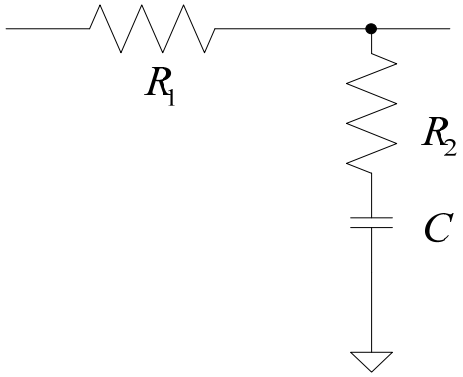
$$H(s)=\frac{\theta_{out}(s)}{\theta_{ref}(s)}=\frac{NK_{PD}K_{VCO}}{s^2NRC+sN+K_{PD}K_{VCO}}$$

$$H(s)=\frac{N\omega_n^{\ 2}}{s^2+2\xi\omega_n s+\omega_n^{\ 2}}$$

$$\omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{NRC}} \qquad \xi=\frac{1}{2}\sqrt{\frac{N}{K_{PD}K_{VCO}RC}}$$

PLL Linear Model

$$F(s)=\frac{1+\tau_2 s}{1+\tau_1 s} \qquad \tau_1=(R_1+R_2)C \qquad \tau_2=R_2C$$



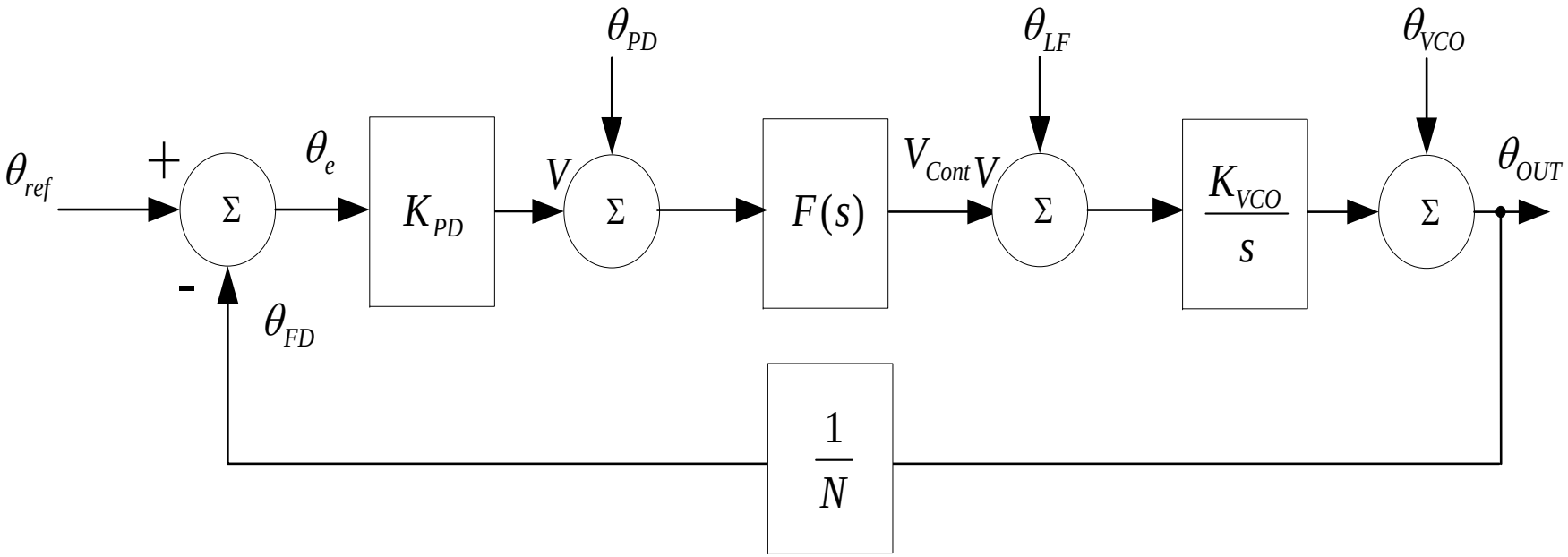
$$H(s)=\frac{s\omega_n(2\xi-\frac{N^2\omega_n}{K_{PD}K_{VCO}})+N\omega_n^{\,2}}{s^2+2\xi\omega_n s+\omega_n^{\,2}}$$

$$\omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}} \qquad \xi=\frac{1}{2}\sqrt{\frac{K_{PD}K_{VCO}}{N\tau_1}(\tau_2+\frac{N}{K_{PD}K_{VCO}})}$$

What Determines Stability and Bandwidth?

- Damping Factor (measure of stability)
- Natural Frequency (measure of bandwidth)
- Damping and natural frequency can be set independently by LPF resistor

Noise Model


θ_{ref}
+
-
Σ
θ_e
K_{PD}
θ_{PD}
V
Σ
$F(s)$
V_{Cont}
θ_{LF}
V
Σ
K_{VCO}
s
θ_{VCO}
Σ
θ_{OUT}
θ_{FD}
$\frac{1}{N}$

Noise Model---Transfer Functions

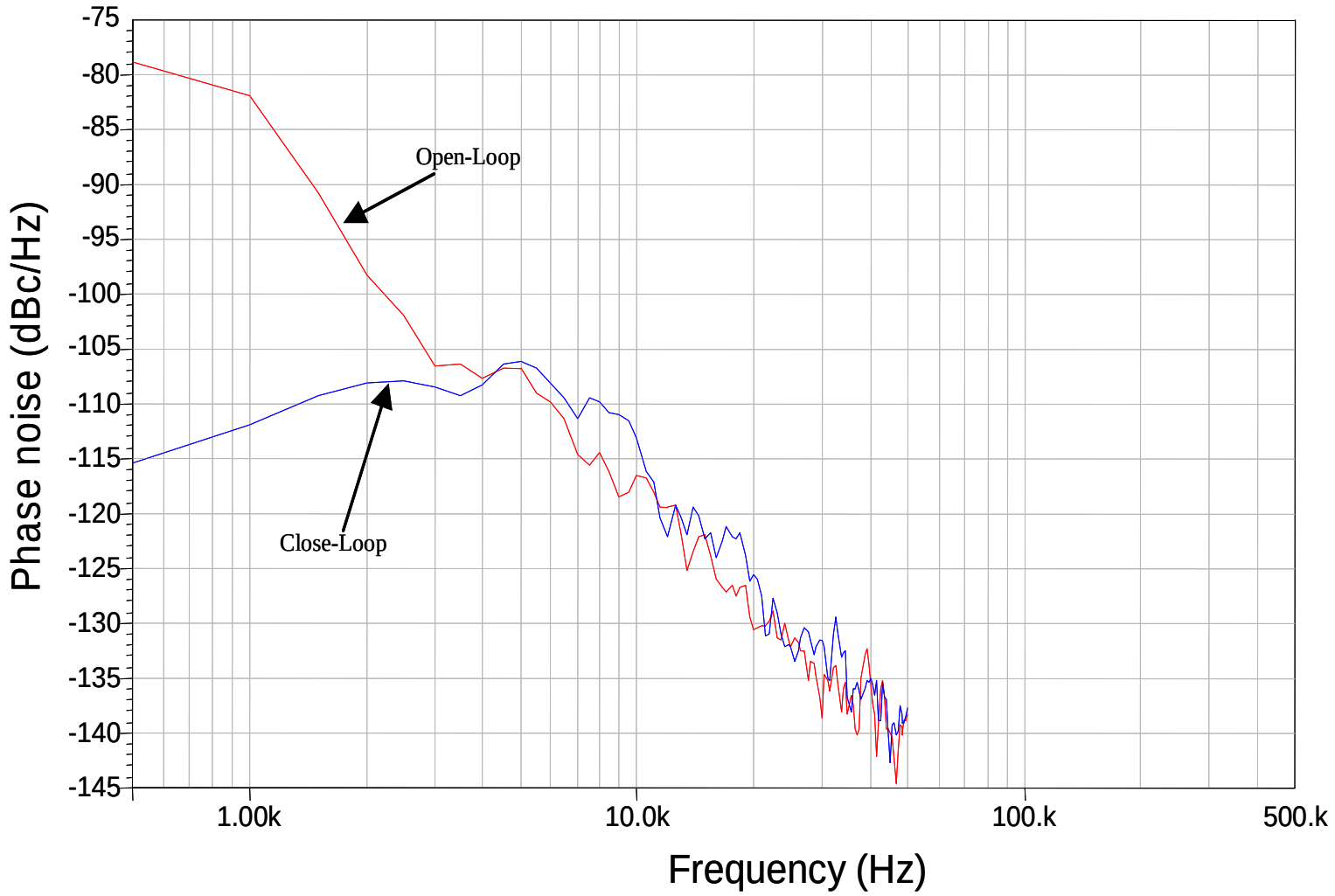
$$H(s)=\frac{\theta_{out}(s)}{\theta_{ref}(s)}=\frac{NK_{PD}K_{VCO}F(s)}{Ns+K_{PD}K_{VCO}F(s)}$$

$$\frac{\theta_{out}(s)}{\theta_{vco}(s)}=\frac{Ns}{Ns+K_{PD}K_{vco}F(s)}$$

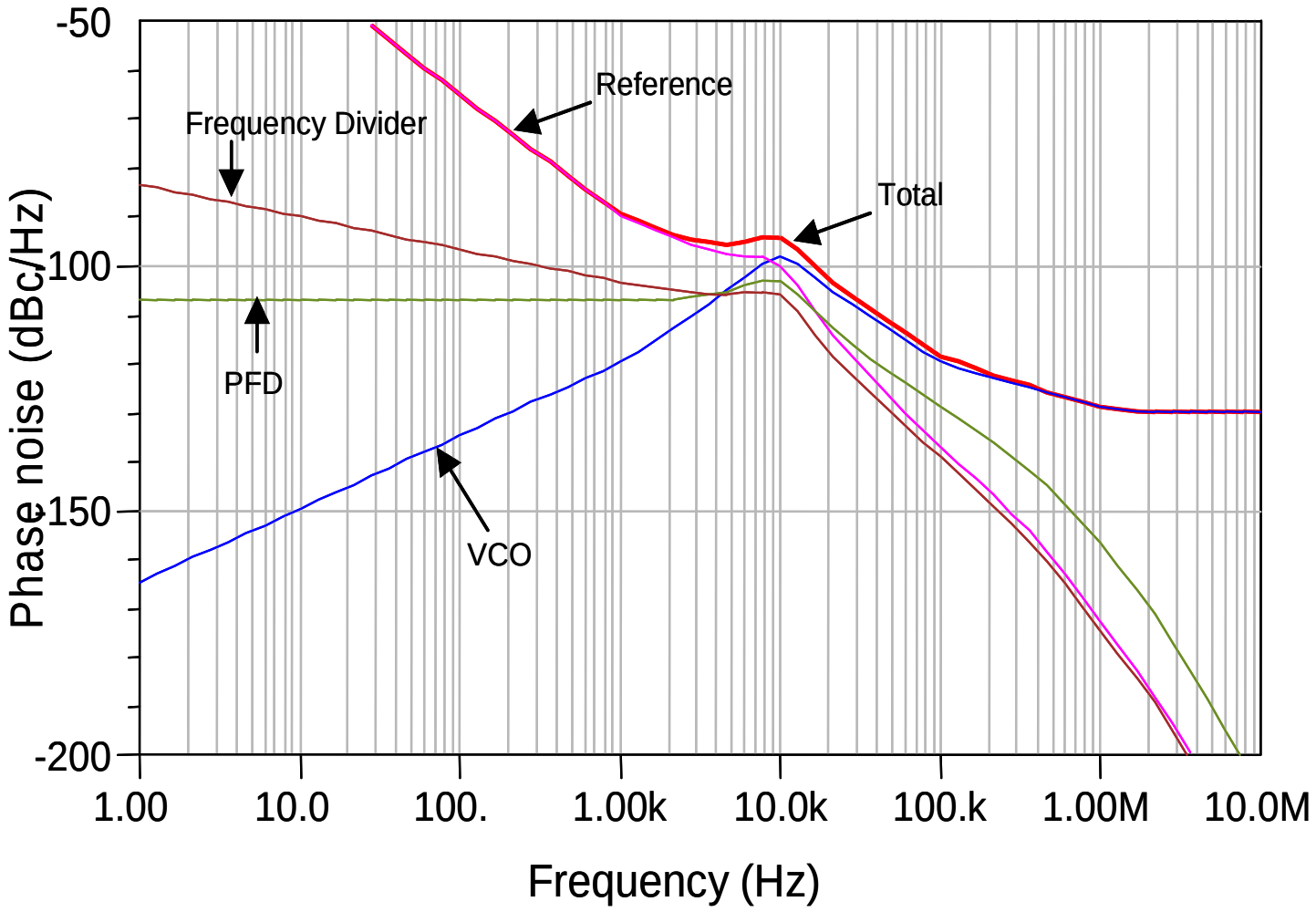
$$\frac{\theta_{out}(s)}{\theta_{vco}(s)}=\frac{Ns}{Ns+K_{pd}K_{lf}K_{vco}}=\frac{s}{s+\omega_c}$$

For $F(s)=K_{lf}$

Noise Model


-75
-80
-85
-90
-95
-100
-105
-110
-115
-120
-125
-130
-135
-140
-145
Phase noise (dBc/Hz)
Open-Loop
Close-Loop
1.00k
10.0k
100.k
500.k
Frequency (Hz)

Noise Model

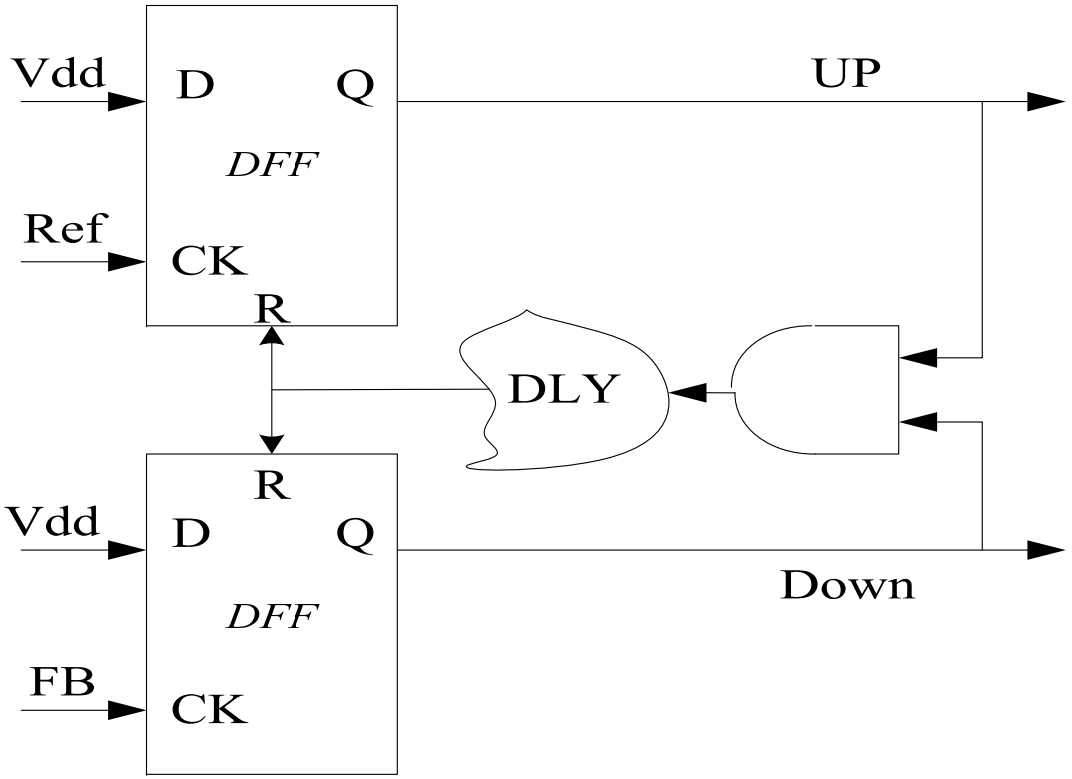

-50
-100
-150
-200
Phase noise (dBc/Hz)
Reference
Frequency Divider
Total
PFD
VCO
1.00
10.0
100.
1.00k
10.0k
100.k
1.00M
10.0M
Frequency (Hz)

PLL Circuits

- Phase-Frequency Detector
- Charge-Pump
- Low-Pass Filter
- Voltage-Controlled Oscillator
- Voltage Regulator

PFD Block Diagram

Edge-triggered - Input duty-cycle doesn't matter
Pulse-widths proportional to phase error

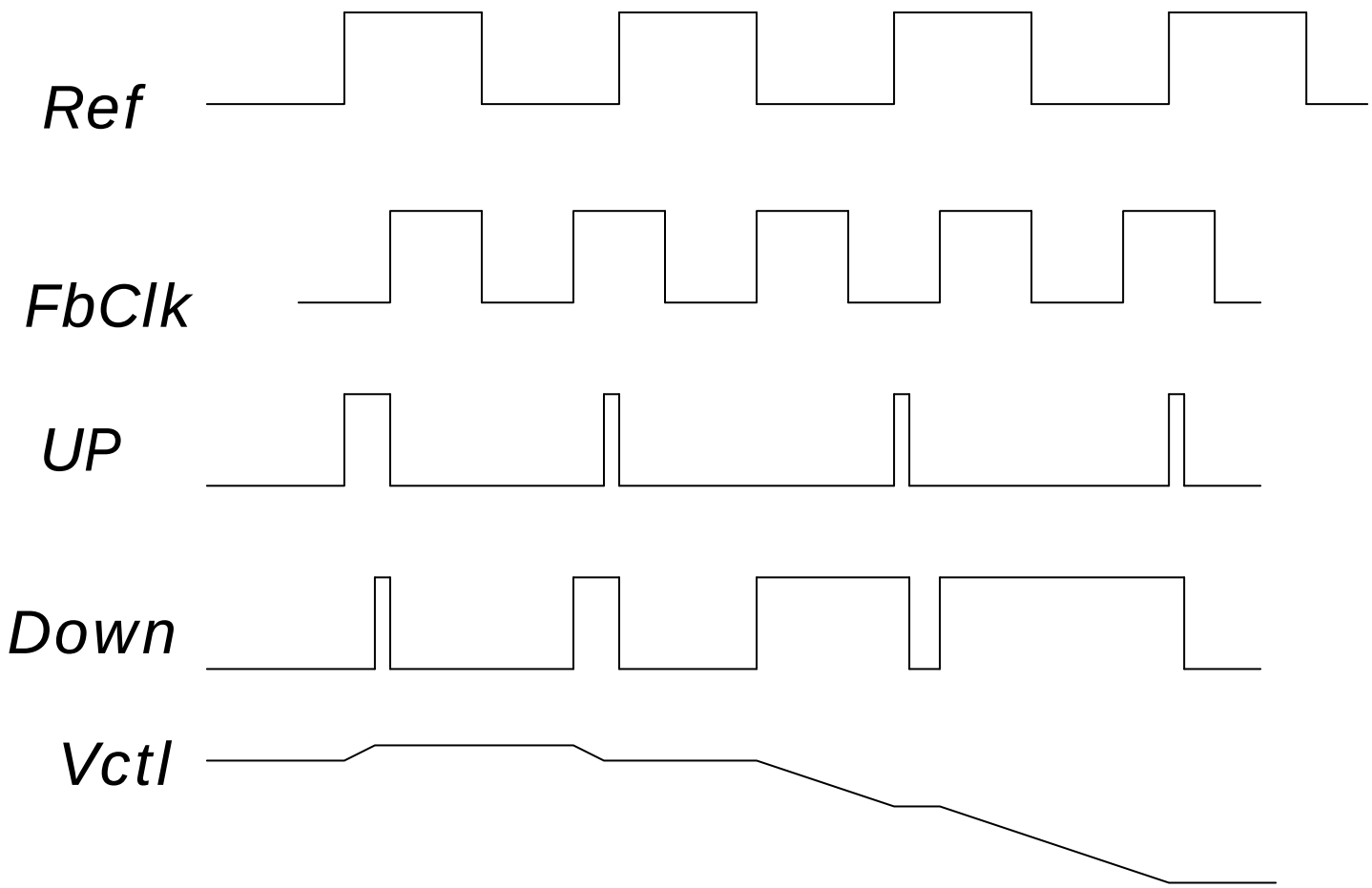


PFD Logic States

3 and “1/2” Output states
States:

UP	Down	Effect:
0	0	No Change
0	1	Slow Down
1	0	Speed Up
1	1	Avoid Dead-Zone

Example: PFD



Avoiding the Dead-Zone

- "Dead-zone" occurs when the loop doesn't respond to small phase errors - e.g. 10 pS phase error at PFD inputs:
  - PFD cannot generate 10 pS wide *UP* and Down pulses
  - Charge-pump switches cannot turn on and off in 10 pS
  - Solution: delay reset to guarantee min. pulse width (typically > 150 pS)

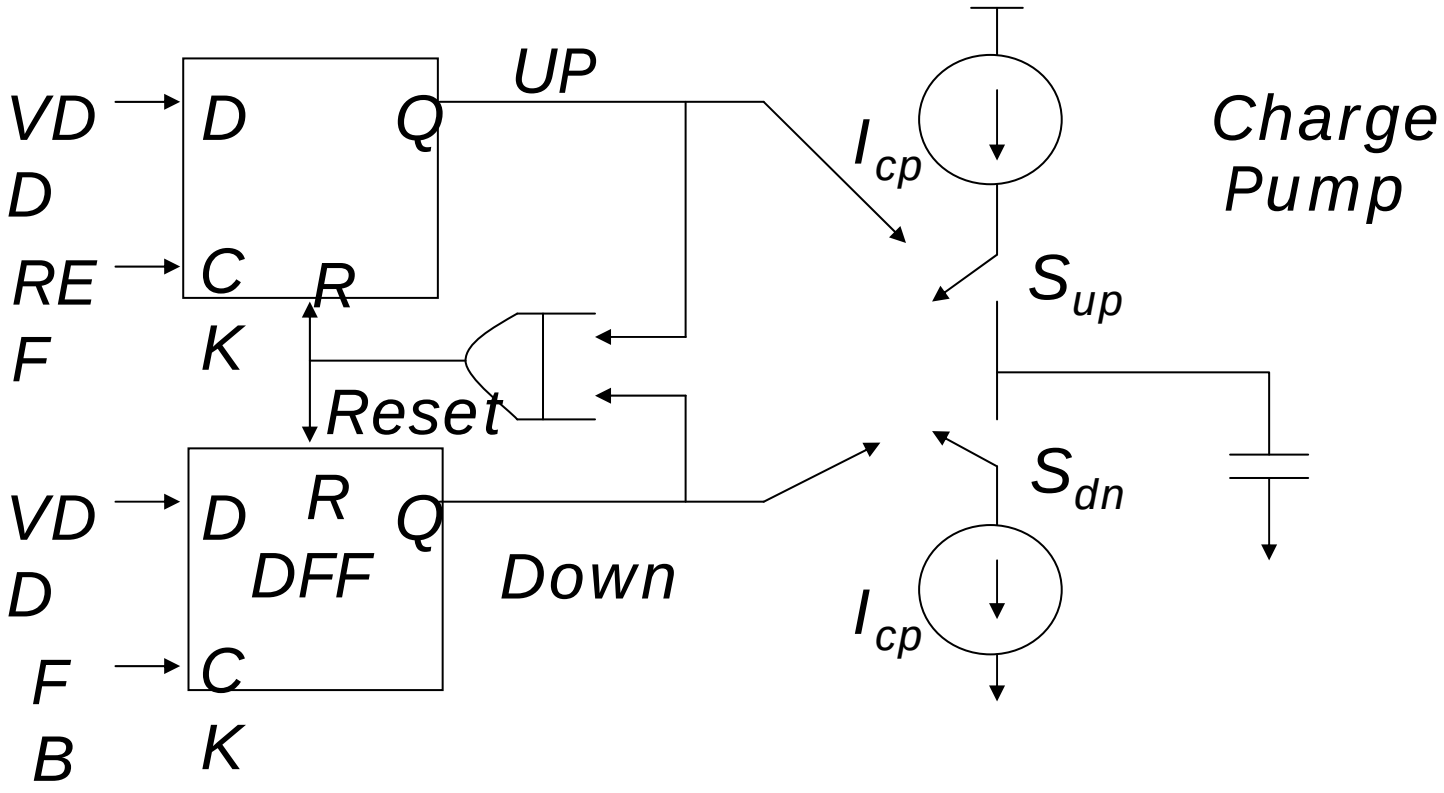
Charge Pump

- Converts PFD phase error (digital) to charge (analog)
- Charge is proportional to PFD pulse widths

$$Q_{cp} = I_{up} * t_{UP} - I_{dn} * t_{Down}$$

- Q_{cp} is filtered/integrated in low-pass filter

Charge Pump


VDD
REF
VDD
FB
D
C
R
K
Q
UP
Reset
DFF
Down
Icp
Icp
Sup
Sdn
Charge Pump

Charge Pump Design Considerations

•Equal *UP/DOWN* currents over entire control voltage range - reduce phase error.
•Minimal coupling to control voltage during switching - reduce jitter.
•Insensitive to power-supply noise and process variations – loop stability.
•Easy-to-design, PVT-insensitive reference current.
•Programmable currents to maintain loop dynamics (vs. M, fref)?
•Typical: 1μA (mismatch)< Icp < 50 μA (ΔVctl)

Static Phase Error and CP Up/Down Mismatches

- Static Phase Error: in lock, net *UP* and *DOWN* currents must integrate to zero
  - If *UP* current is 2X larger, then *DOWN* current source must be on 2X as long to compensate
  - Feedback clock must lead reference for *DOWN* to be on longer
  - Terr = Tdn - Tup = Treset * (Iup/Idn – 1)

Static Phase Error and CP Up/Down Mismatches

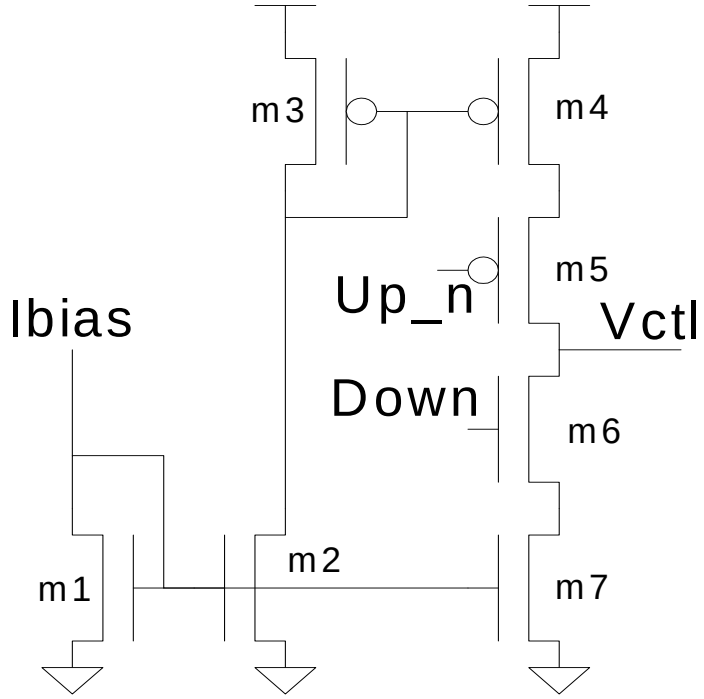
- Phase error can be extremely large at low VCO frequencies (esp. if self-biased) due to mismatch in current mirrors (low V_{gs}-V_t)
- Increase V_{gs} or decrease ΔV_t (large W*L)
- Typical static phase error < 100 pS

VCO Jitter and CP Up/Down Mismatches

•PFD-CP correct at rate of reference (e.g. 10nS).
•Most phase error correction occurs near reference rising edge and lasts < 200 pS, causing a control voltage ripple.
•This ripple affects the VCO cycles near the reference more than VCO cycles later in the ref cycle, causing VCO jitter.
•Typ. Jitter << 1% due to *Up/Down* Mismatches
•Avoid ripple by spreading correction over entire ref cycle. (Maneatis JSSC ’03)

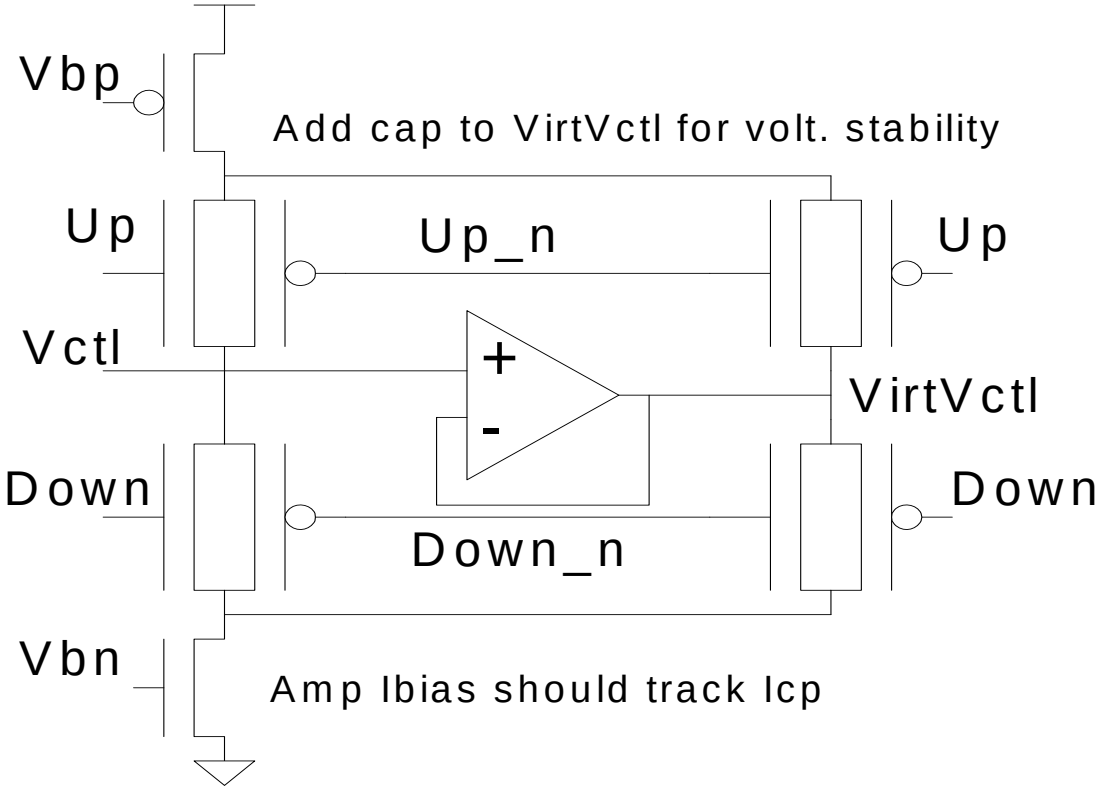
Simple Charge Pump

- R(switches) varies with *Vctl* due to body-effect
- Use CMOS pass-gate switches for less *Vctl* sensitivity
- Long-channel current sources for matching and higher Rout



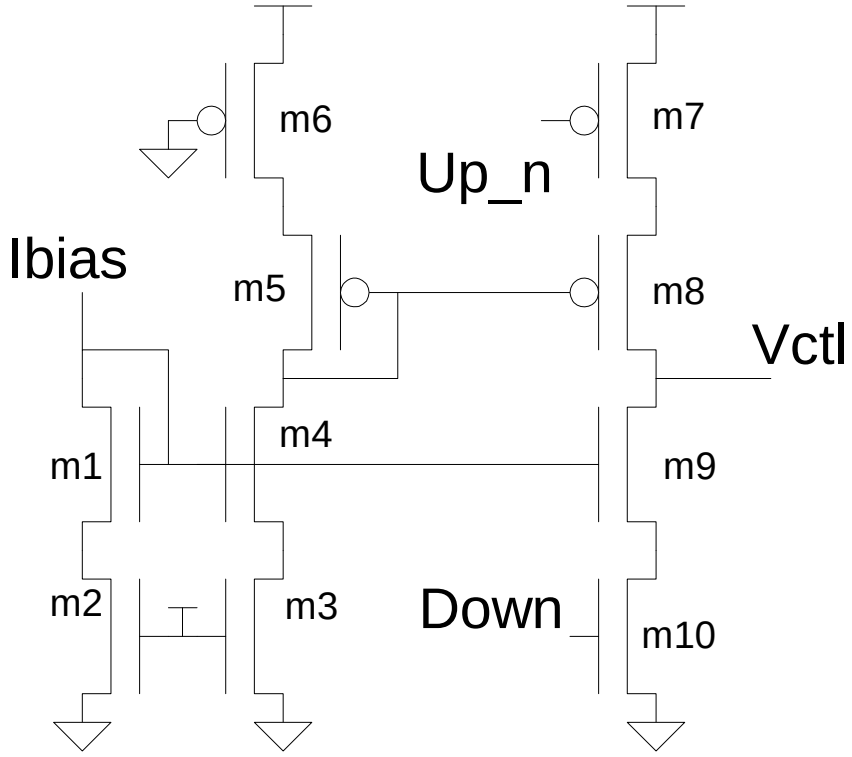
Charge Pump: const I with amp

Amp keeps Vds of current sources constant (Young '92)
Amp sinks "waste" current when UP, DOWN off



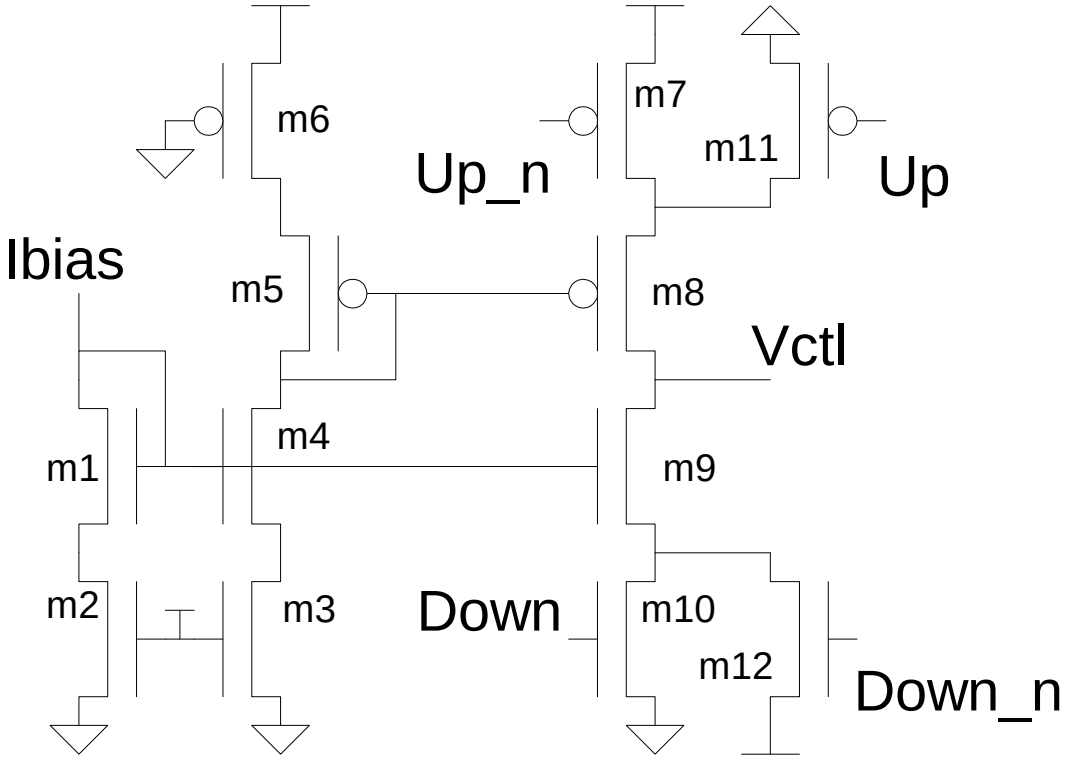
Charge Pump – switches reversed

•Switches closer to power rails reduce noise and *Vctl* dependence → Icp not constant with up/down



m1,m4,m5,m8,m9: long L

Charge Pump: switches reversed with fast turn-off



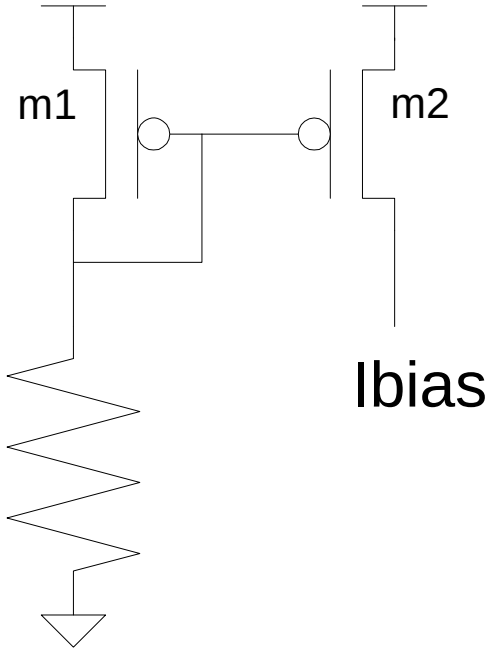
m1,m4,m5,m8,m9: long L

m11, m12: faster turn-off

(Ingino '01)

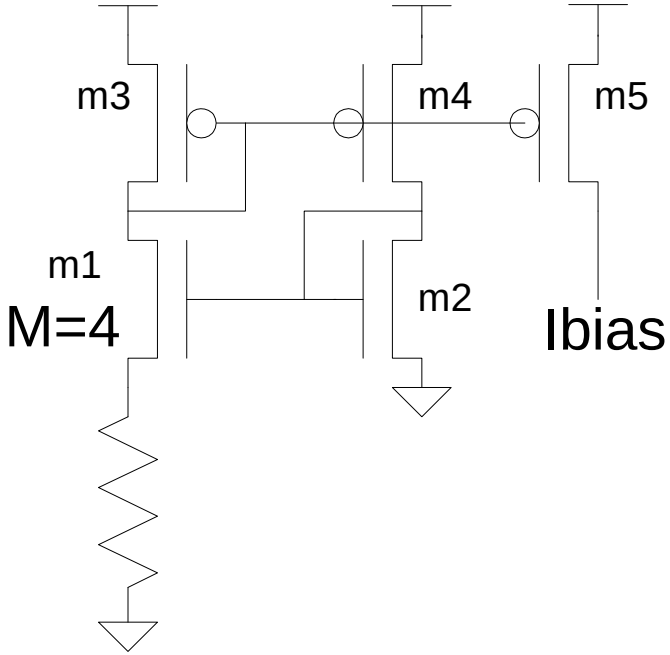
Simple Charge-Pump Bias

- Ib ~ (Vdd – Vt)/R
- Ib dependent on PVT
- Prefer low-Vt, moderate-to-long L for process insensitivity, large W/L for low gate-overdrive
- Pro: Simple, stable. Con: Vdd dependence



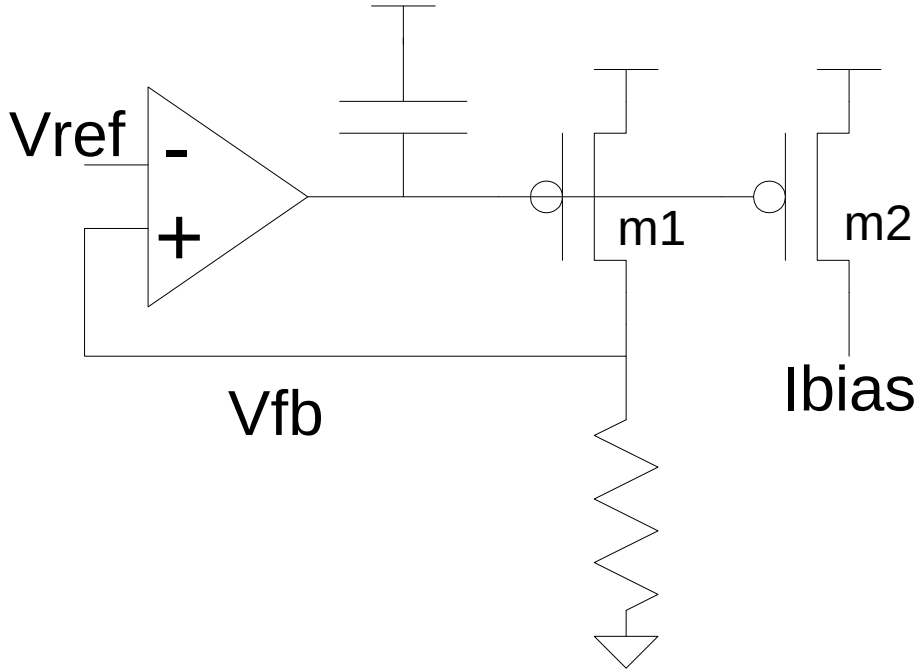
VDD-Independent Ibias

- Ib ~ 1/R2
- Con: requires start-up circuit not shown



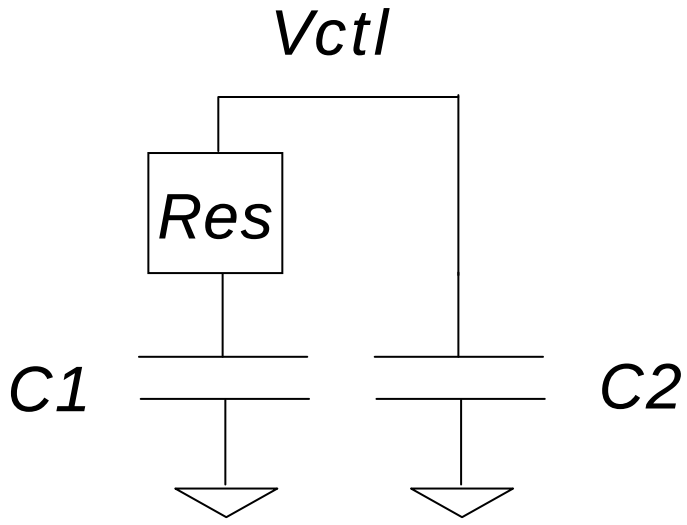
Bandgap-Based Ibias

- Ib ~ Vref/R
- Con: feedback loop may oscillate
  - cap added to improve stability
- Pro: VDD-independent, mostly Temp independent



Low-Pass Filter

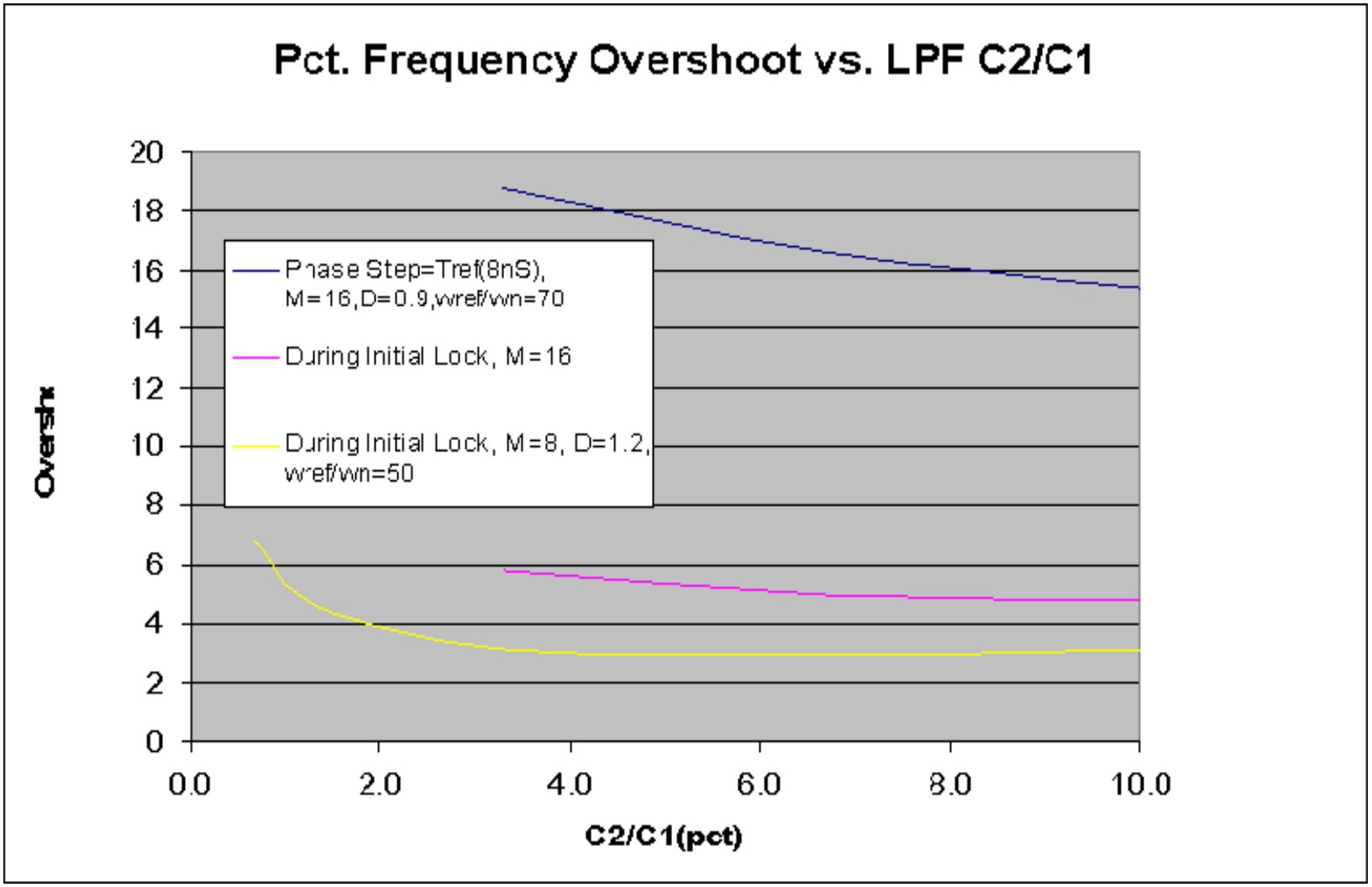
•Integrates charge-pump current onto C1 cap to set average VCO frequency (“integral” path).
•Resistor provides instantaneous phase correction w/o affecting avg. freq. (“proportional” path).
•C2 cap smoothes large IR ripple on Vctl
•Typical value: 0.5k < Rlpf < 20kOhm



Low-Pass Filter Smoothing Cap(C_2)

- "Smoothing" capacitor on control voltage filters CP ripple, but may make loop unstable
- Creates parasitic pole: $\varpi p = 1/(R\ C2)$
- $C2 < 1/10 * C1$ for stability
- $C2 > 1/50 * C1$ for low jitter
- Smoothing cap reduces "IR"-induced VCO jitter to < 0.5% from 5-10%
- $\Delta fvco = KvcoIcpTerr/C2$
- Larger C2/C1 increases phase error slightly

Low-Pass Filter Smoothing Cap(C_2)



Low-Pass Filter Capacitors

- Even thick gate oxide may still leak too much
- Large filter cap (C_1) typically ranges from 50pF to 400 pF
- C_1 cap BW may be as low as ~10X PLL BW for nearly ideal behavior
- Min C_2 BW set by T_{ref}
- Cap BW ~ $1/RC \sim 1/L^2$
- Gate cap not constant with V_{gs}

PLL Suppression of VCO Noise

- PLL acts like a high-pass filter in allowing VCO noise to reach PLL output
- Need noise-immune VCO to minimize jitter
  - Feedback loop cannot react quickly.
- Power-supply noise is largest source of VCO noise

VCO Design Concerns

- Large frequency range to cover PVT variation:
- Single-ended or differential?
- Vco gain (fvco = Kvco* Vctl) affects loop stability
- More delay stages → easier to initiate oscillation
  - Gain(DC) > 2 for 3 stages
  - Gain(DC) > sqrt(2) for 4 stages

Voltage Regulator/Filter

- Used to filter power-supply noise
  - typically > 20 dB (10x) PSRR over entire frequency range
  - desire 30+ dB
- Secondary purpose is to set precise voltage level for PLL power supply
  - usually set by bandgap reference

Bandgap Reference w/Miller Cap

•Stability and PSRR may be poor w/o Miller cap
•Miller cap splits poles. Can also add R in series w/Cc for more stability (Razavi ’00)