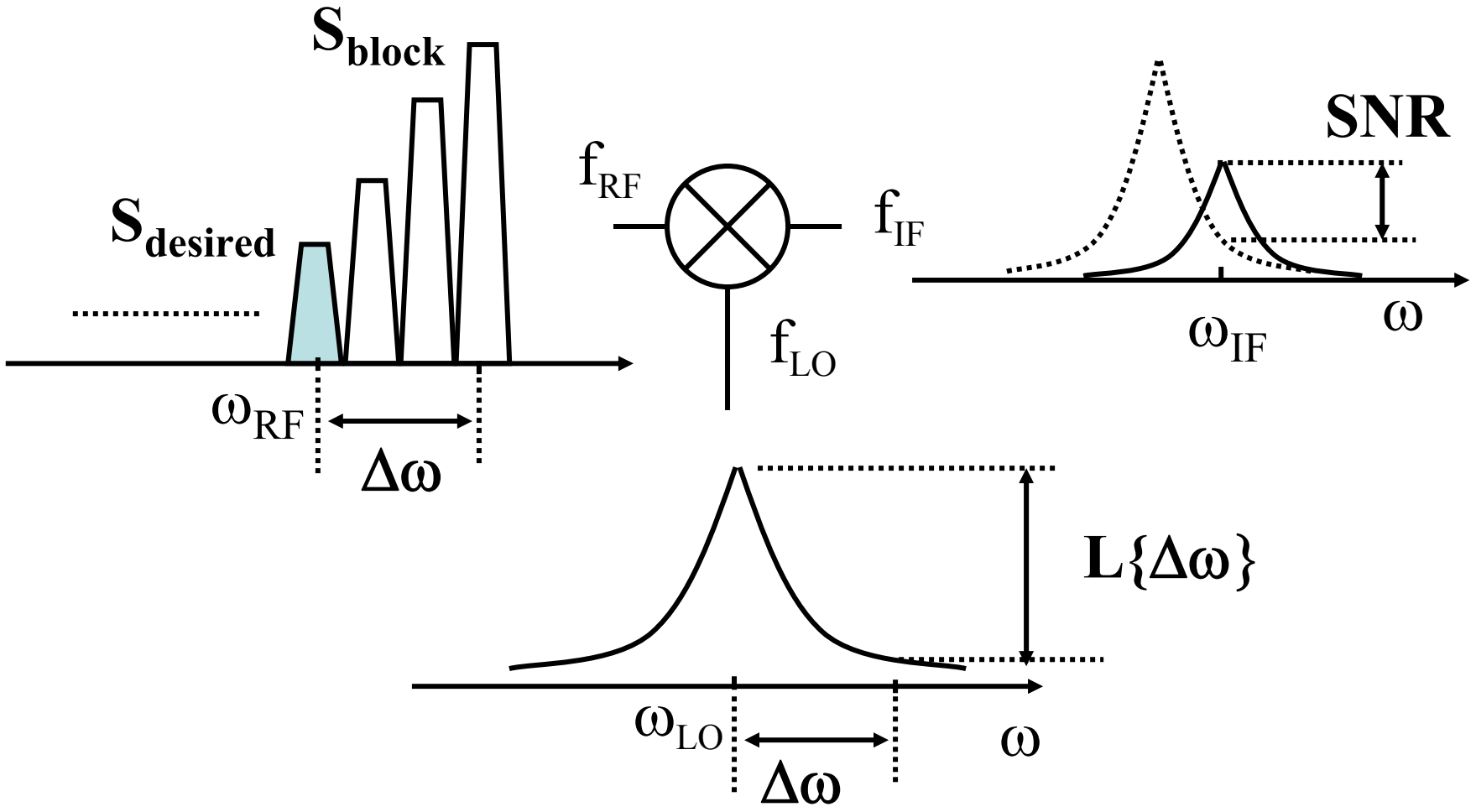
Introduction to CMOS RF Integrated Circuits Design

V. Voltage Controlled Oscillators

Outline

- Phase Noise and Spurs
- Ring VCO
- LC VCO
- Frequency Tuning (Varactor, SCA)
- Phase Noise Estimation
- Quadrature Phase Generator

VCO Phase Noise



Phase Noise Requirement

$$SNR = S_{desired} - S_{noise}$$

$$= S_{desired} - [S_{block} + L\{\Delta\omega\} + 10\log(f_{ch})]$$

$$\therefore L\{\Delta\omega\} < S_{desired} - S_{block} - SNR_{\min} - 10\log(f_{ch})$$

$$Ex:\ GSM$$

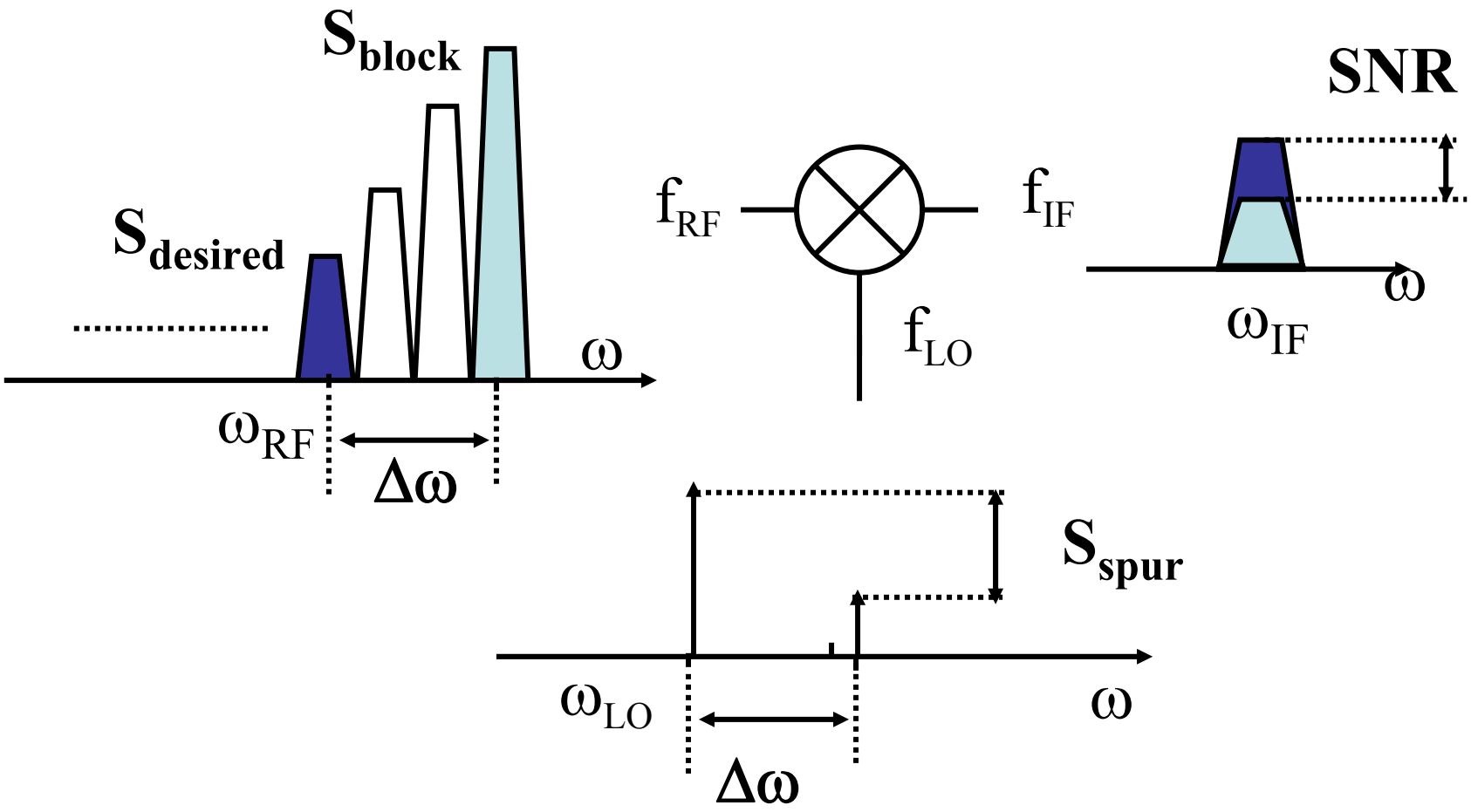
$$S_{desired} = -102dB;\ S_{block} = -23dB\ @\ 600KHz$$

$$SNR_{\min} = 9dB;\ f_{ch} = 200KHz$$

$$\because L\{\Delta\omega\} < -102 + 23 - 9 - 10\log(200K)$$

$$< -141dBc/Hz\ @\ 600KHz$$

Spurious-Tone Performance



Spurious-Tone Requirement

$$SNR = S_{desired} - S_{noise}$$
$$= S_{desired} - (S_{block} + S_{spur})$$
$$\therefore S_{spur} < S_{desired} - S_{block} - SNR_{\min}$$

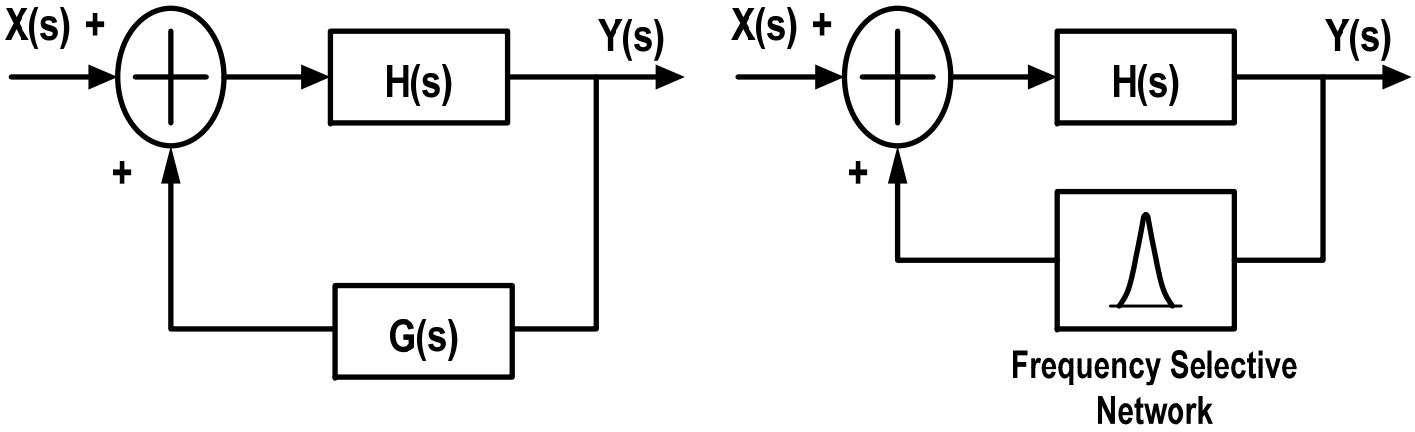
Ex: GSM

$$S_{desired} = -102dB;\ S_{block} = -23dB@600KHz$$
$$SNR_{\min} = 9dB;$$
$$\because S_{spur} < -102 + 23 - 9 = -88\,dBc$$

Typical Figure of Merits for VCO

Frequency	~ 1 – 5 GHz
Tuning Range	~ 10 – 20 %
Phase Noise	- 105 dBc/Hz @ 100 KHz
Supply Voltage	~ 1.5 V
Current	< 10 mA

Oscillation Theory



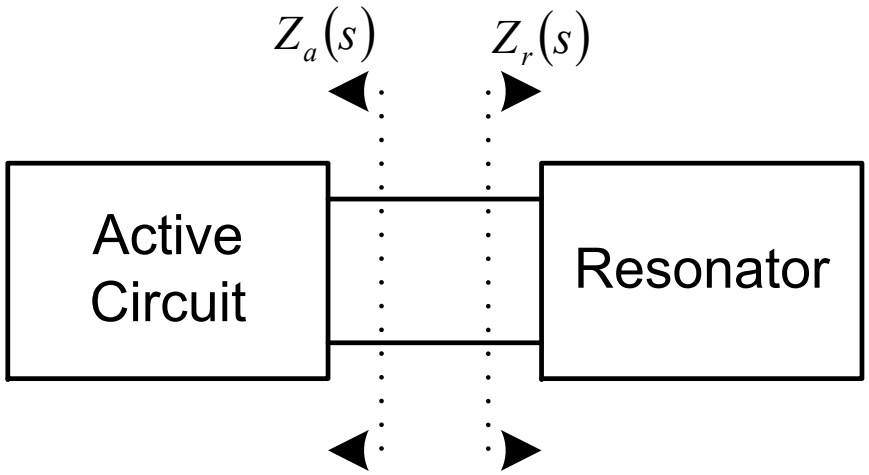
$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)G(s)}$$

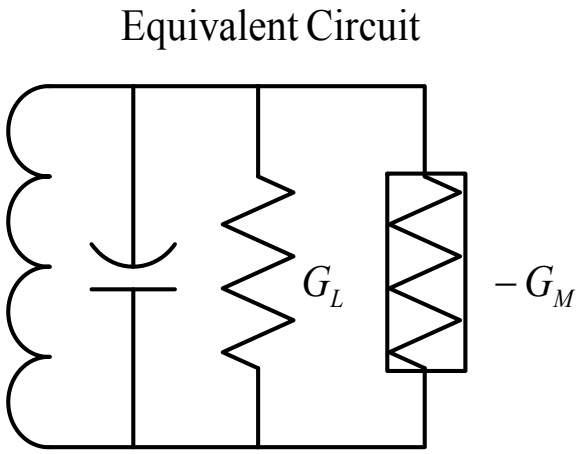
For steady oscillation, Barkhausen's criteria must be simultaneously met:

$$\left|H(s)G(s)\right| \geq 1$$

$$\angle H(s) + \angle G(s) = 2n\pi$$

Negative Resistance Model

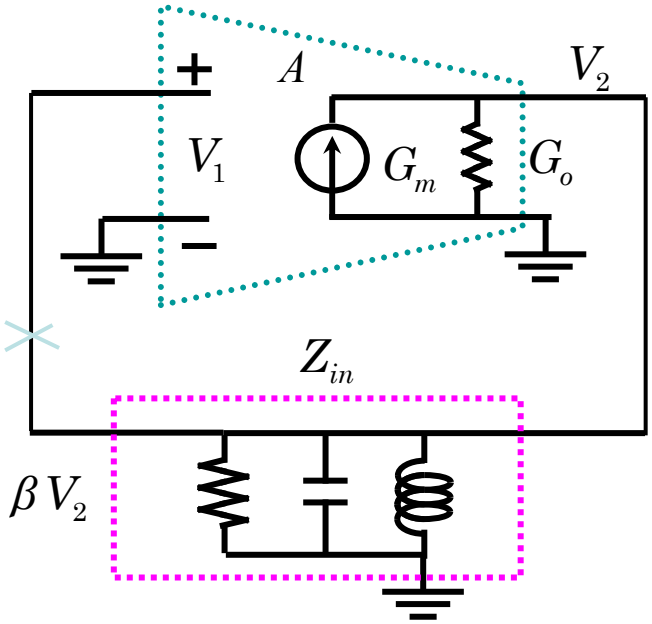




During Oscillation:

$$\mathrm{Re}\left[Z_a(s)\right] + \mathrm{Re}\left[Z_r(s)\right] = 0$$

Negative Resistance Model



$$A = \frac{G_m Z_{in}}{1 + G_o Z_{in}}$$

$$Y = \frac{1}{Z_{in}} + G_o - G_m\beta = \left(\frac{1}{Z_{in}} + G_o\right)(1 - A\beta)$$

→ Determine the oscillation frequency

$$\mathrm{Im}(Y) = 0$$

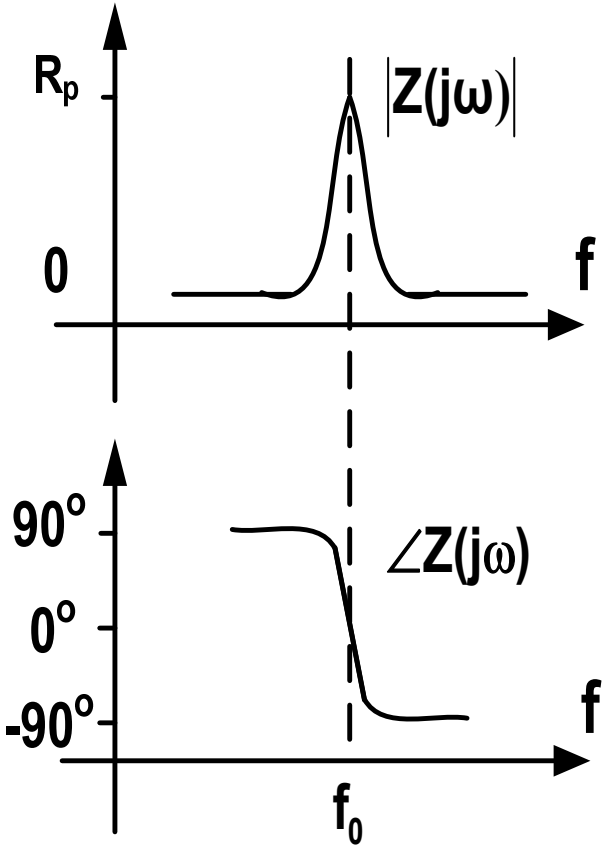
$$\mathrm{Im}(1 - A\beta) = 0$$

Oscillation:

$$A\beta > 1 \Leftrightarrow \mathrm{Re}\left[\left(\frac{1}{Z_{in}} + G_o\right)(1 - A\beta)\right] < 0$$

Negative Conductance

Negative Resistance Model



$$f_o = \frac{1}{2\pi\sqrt{L\ C}}$$

Ring vs LC Oscillators

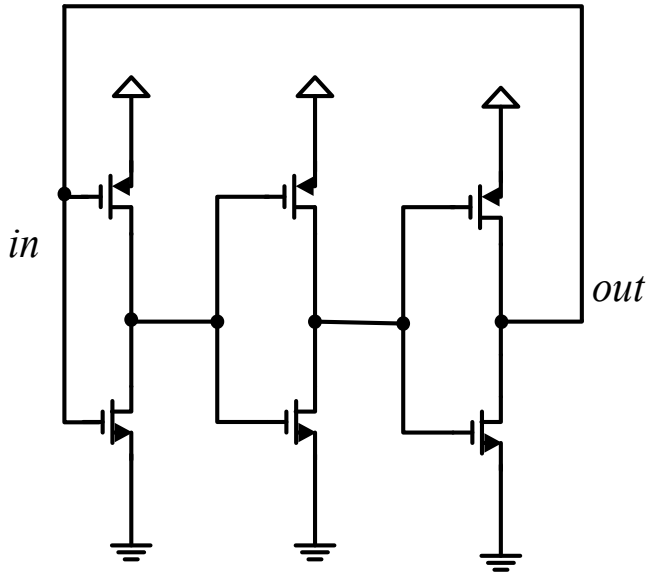
Parameters	Ring VCO	LC VCO
Phase Noise	Poor	Good
Tuning Range	Large	Small
Power Consumption	High	Low
Chip Area	Small	Large
Output Waveform	Square	Sinusoidal

Ring VCO

- A Cascade of Delay Cells Connected in Feedback to Meet Oscillation Criteria (Barkhausen)
  - Loop Gain @ $w_{osc} > 1$
  - Total Phase Shift @ $w_{osc} = 2n\ \pi$
- For Single-Ended Design, Needs An Odd Number of Delay Cells to provide $2n\ \pi$ phase shift

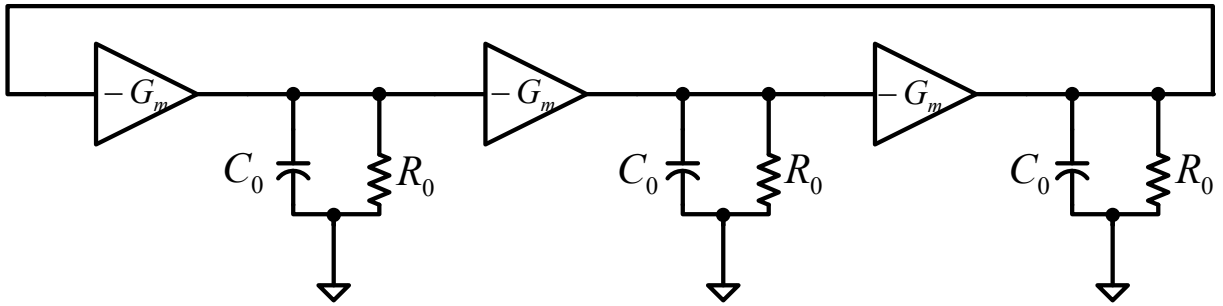
$$f_{osc} = \frac{1}{2N\tau_d}$$

Implementation of Ring Oscillator



$$H(j\omega_0) = \left(\frac{-GmR_0}{1 + j\omega_0 R_0 C_0}\right)^N$$

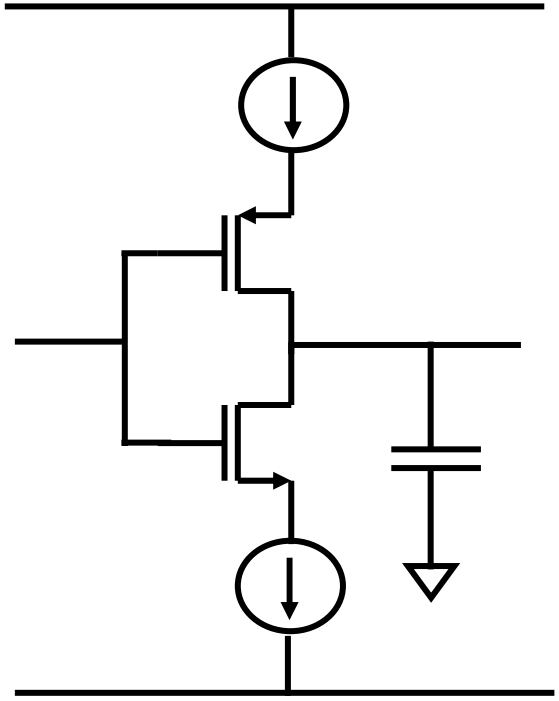
$$f_{osc} = \frac{1}{2N\tau_d}$$

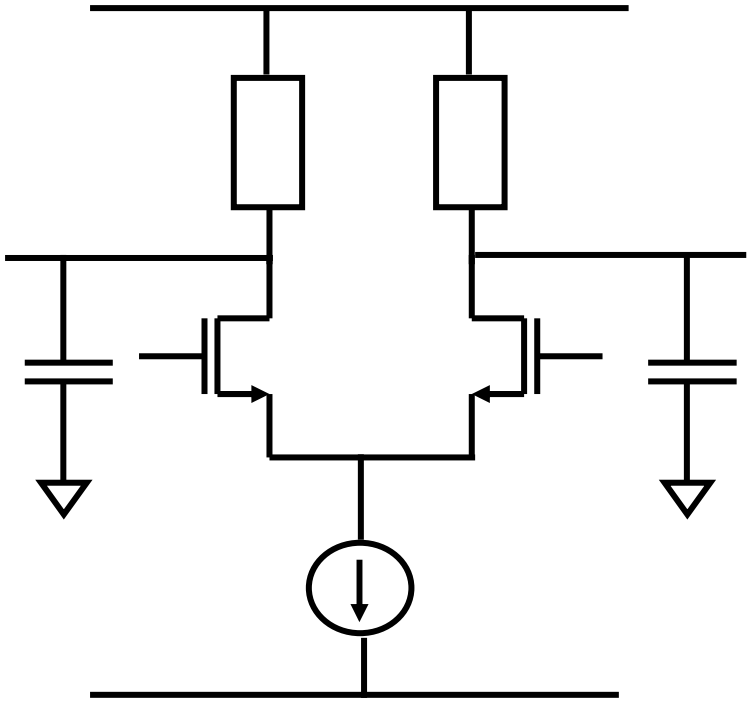


Ring VCO

- Delay Cells Can Simply Be Digital or Analog Inverters
- Delay and Frequency Can Be Tuned By Bias Current, Device Transconductance, or Loading Resistance or Capacitance
- Can Provide Rail-To-Rail Output Waveform and Wide Tuning Range
- All Components Contribute Phase Noise

Delay Cells





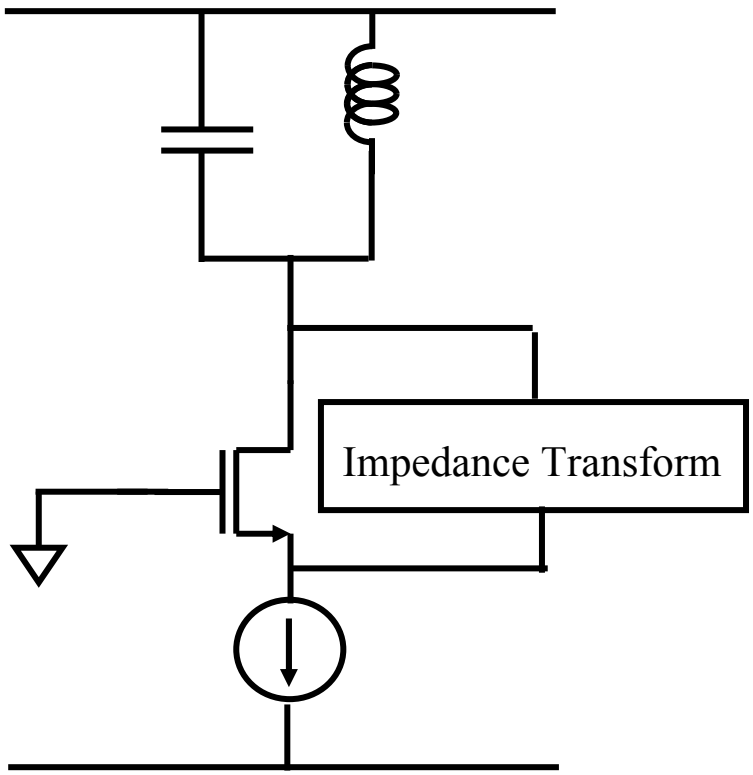
Ring VCO – Differential Design

- Signal is Increased by 6 dB while Noise is Increased by 3 dB => Phase Noise is Improved by 3 dB
- Common-Mode Rejection (Supply, Even-Order Harmonics, Common-Mode, Substrate Noise)
- Double Power, Double Chip Area

LC VCO – Single-Ended Design

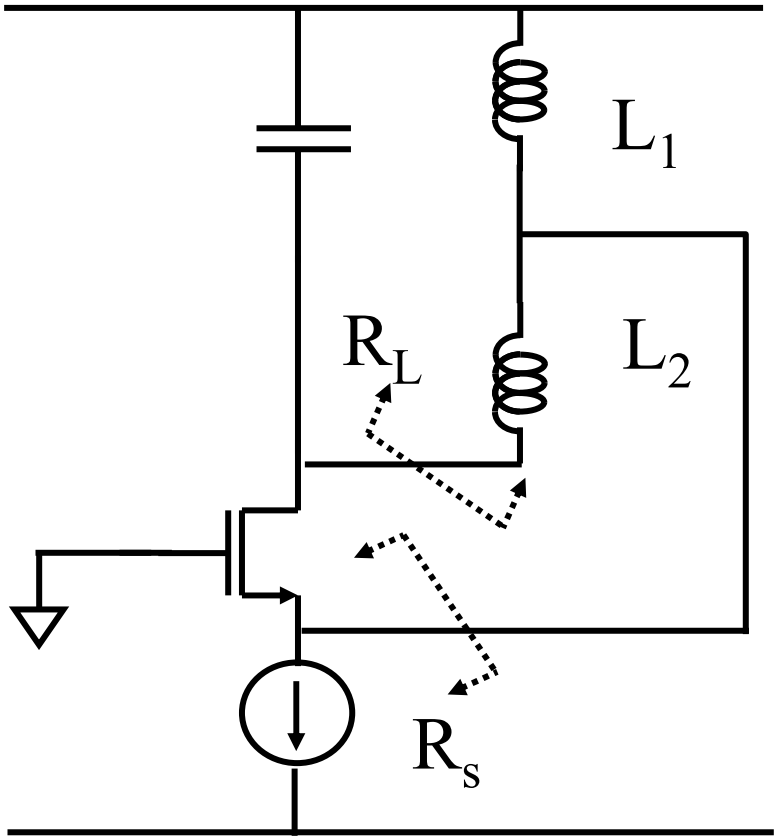
- Use Feedback Principle for Oscillation:
  - Loop Gain @ $w_{osc} > 1$
  - Total Phase Shift @ $w_{osc} = 2n\,\pi$
- Critical to Include Impedance Transform:
  - Not to Degrade Tank Q
  - Improve Gain for Oscillation
- Either Capacitive or Inductive Divider Can Be Used for Impedance Transformation

LC VCO – Single-Ended Design



Feedback can be from drain to source or gate to source

LC VCO – Single-Ended Design

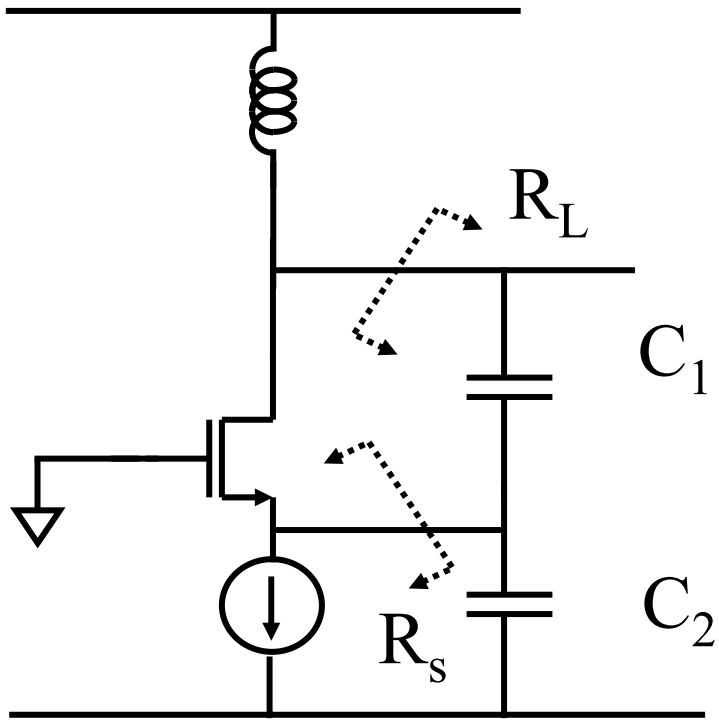


$$f_o = \frac{1}{2\pi\sqrt{(L_1+L_2)C}}$$

$$R_L = R_s\left(1+\frac{L_2}{L_1}\right)^2$$

Hartley Oscillator

LC VCO - Single-Ended Design



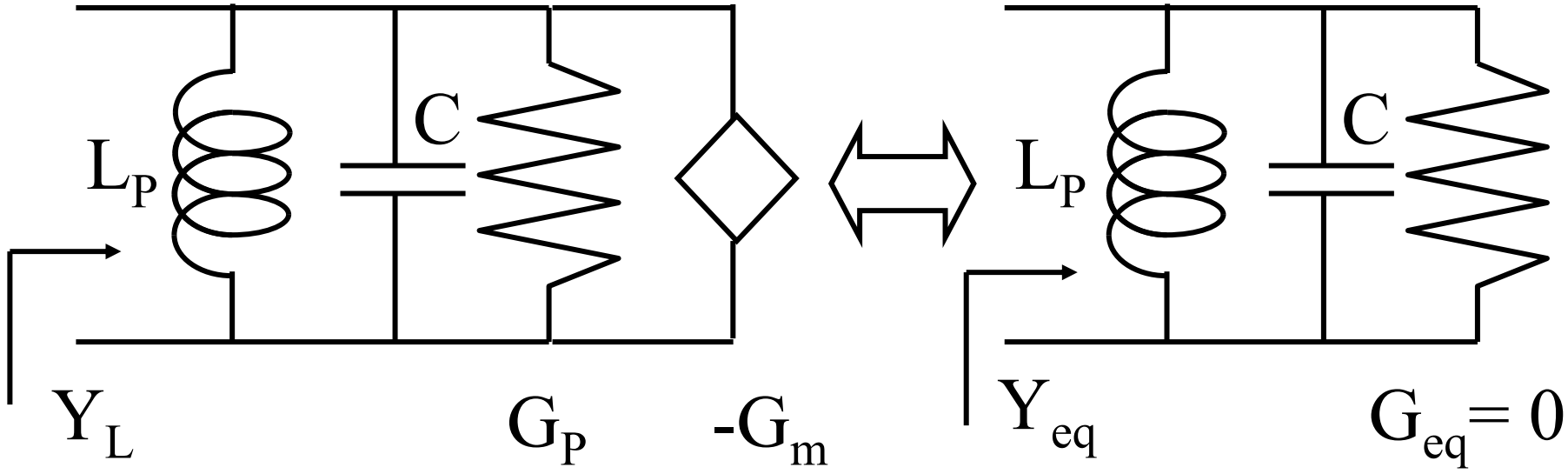
$$f_o = \frac{1}{2\pi\sqrt{L\cdot\left(\frac{C_1\cdot C_2}{C_1+C_2}\right)}}$$

$$R_L = R_s\left(1+\frac{C_2}{C_1}\right)^2$$

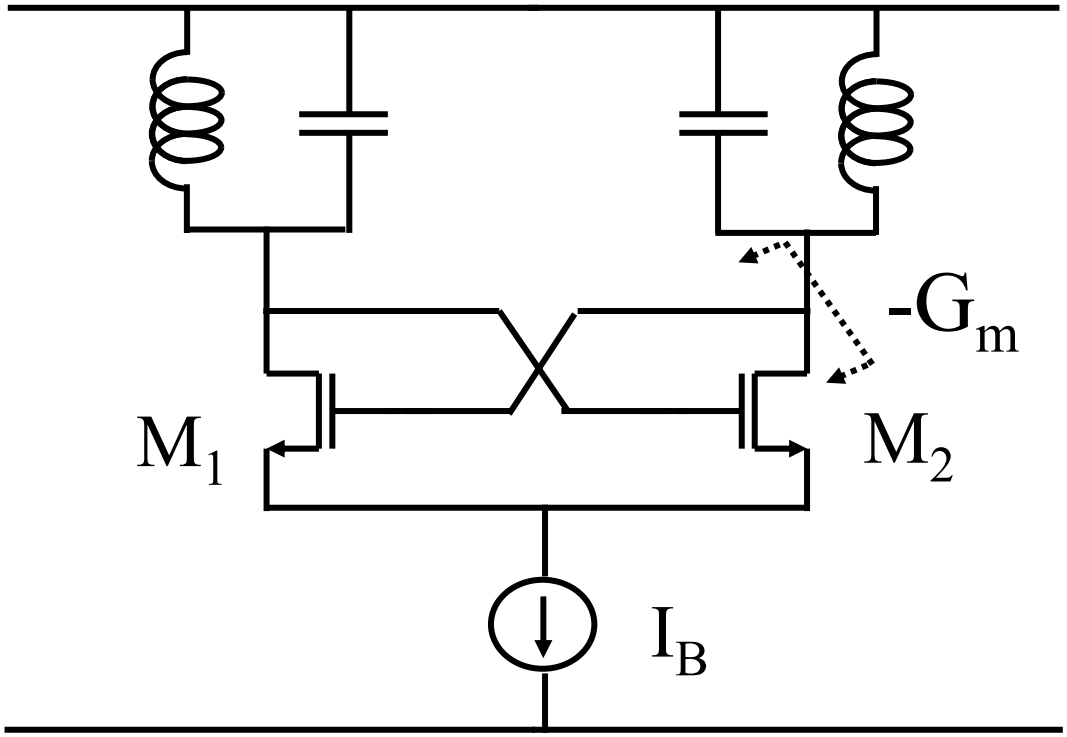
Colpitts Oscillator

LC VCO – Negative Resistance Design

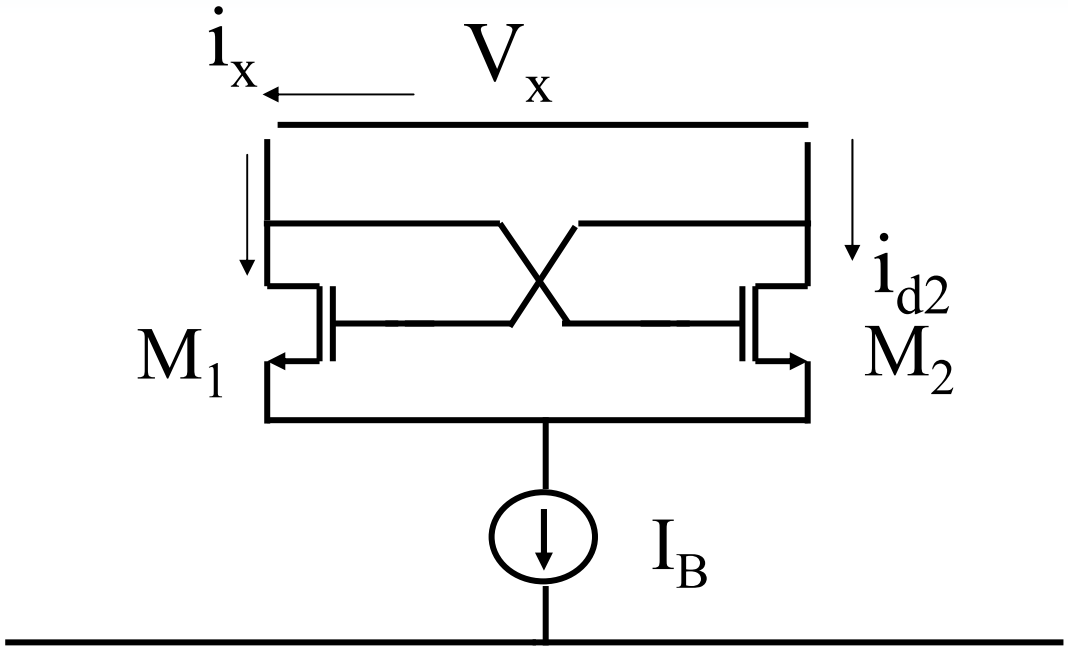
- Make Use of LC Resonant Tank
- Use Negative-Gm Compensation Technique to Achieve Infinite Q for Oscillation



Negative Resistance



Negative Resistance

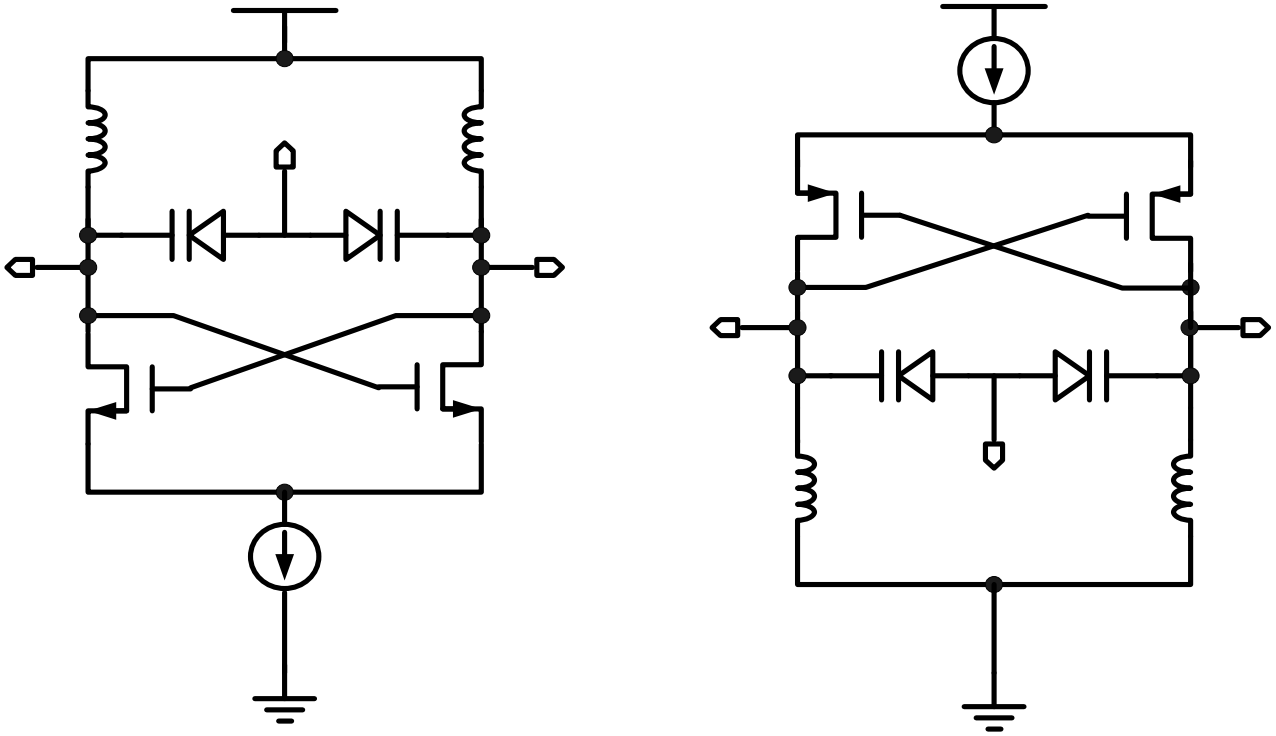


$$i_x = i_{d2} = -i_{d1} \qquad v_x = V_{gs2} - v_{gs1}$$

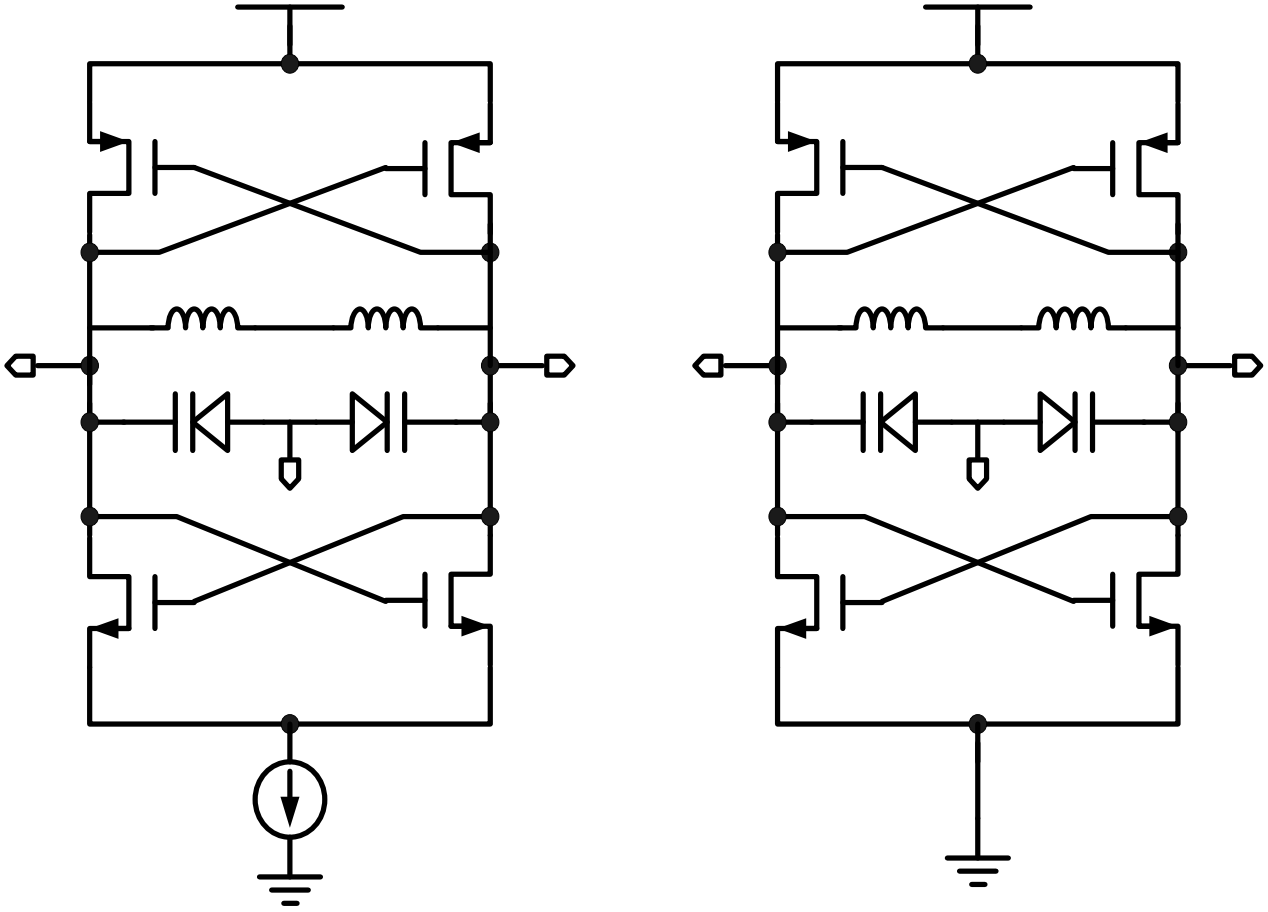
$$i_x = -G_m v_x = -\frac{g_m}{2} v_x$$

At high-frequency the device capacitance and input resistance should be included in the analysis.

Differential VCO



Differential VCOs

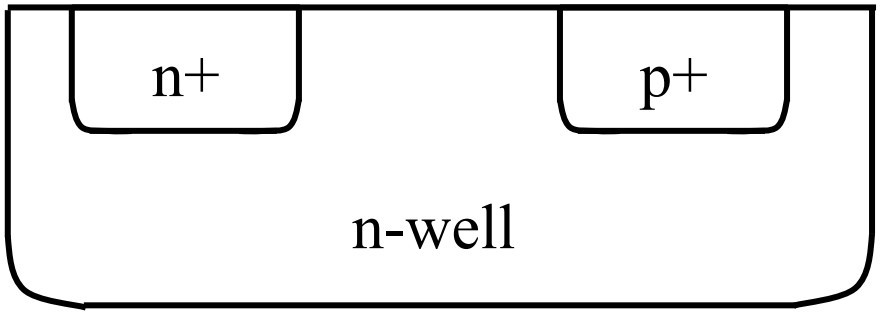


LC VCO – Frequency Tuning

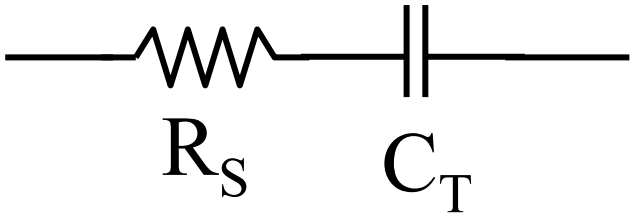
$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

- Frequency Tuning Can Be Achieved By Tuning Capacitance Using a Varactor or a Switchable Capacitor Array (SCA)
- Or Effective Inductance

PN-Junction Varactor

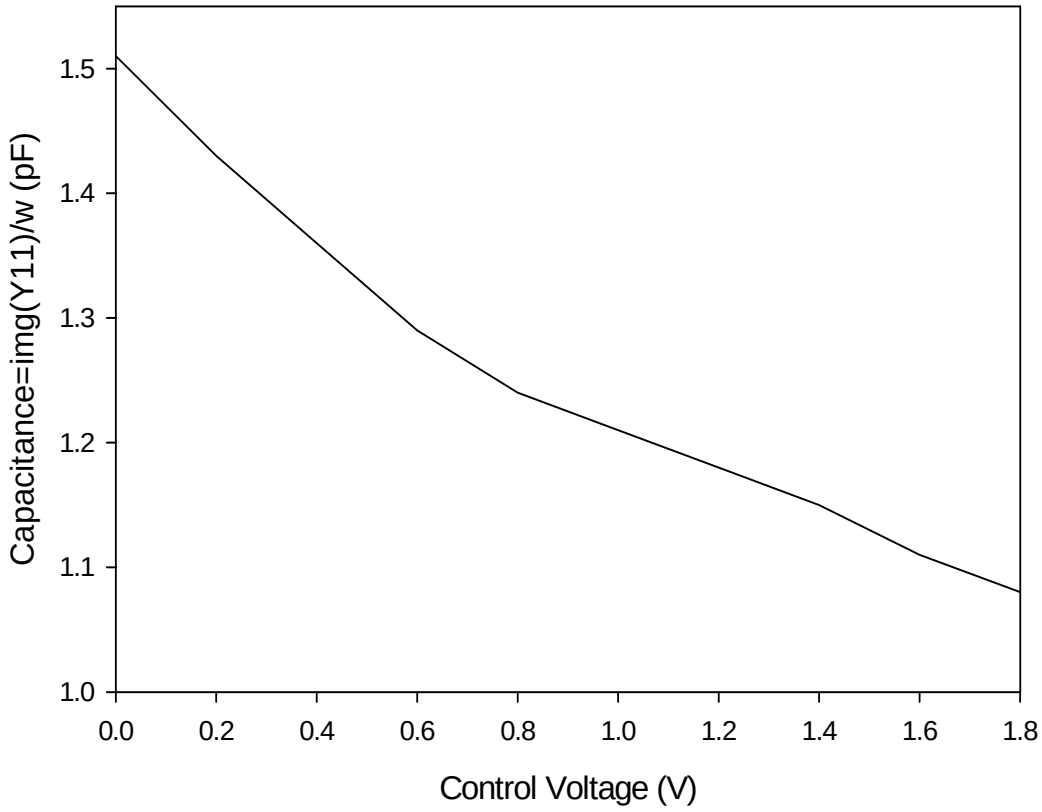


$$C_T = A\frac{C_{jo}}{\sqrt{1-\frac{V_B}{\phi_F}}}$$



$$Q_C = \frac{1}{\omega R_S C_T}$$

PN-Junction Varactor

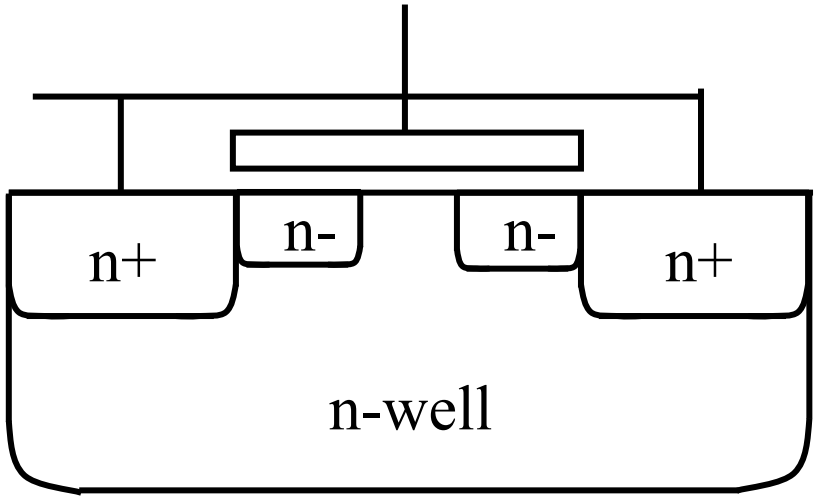


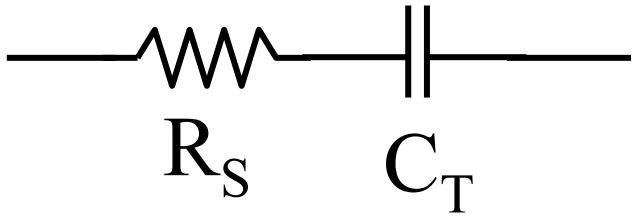
PN-Junction Varactor

- Make Use of Depletion Capacitance of p-n Diode Junction
- n+ Contacts Are Used to Minimize Contact Resistance and thus to Maximize Q
- Reducing Size of p+ Would Minimize p+ Series Resistance

- Increasing Size of p+ Would Increase Number of Contacts and Reduce Contact Resistance
- Measurements Indicate Contact Resistance Dominates => Larger Size of p+ Diffusion is Desired for Higher Q

Accumulation-Mode Varactor

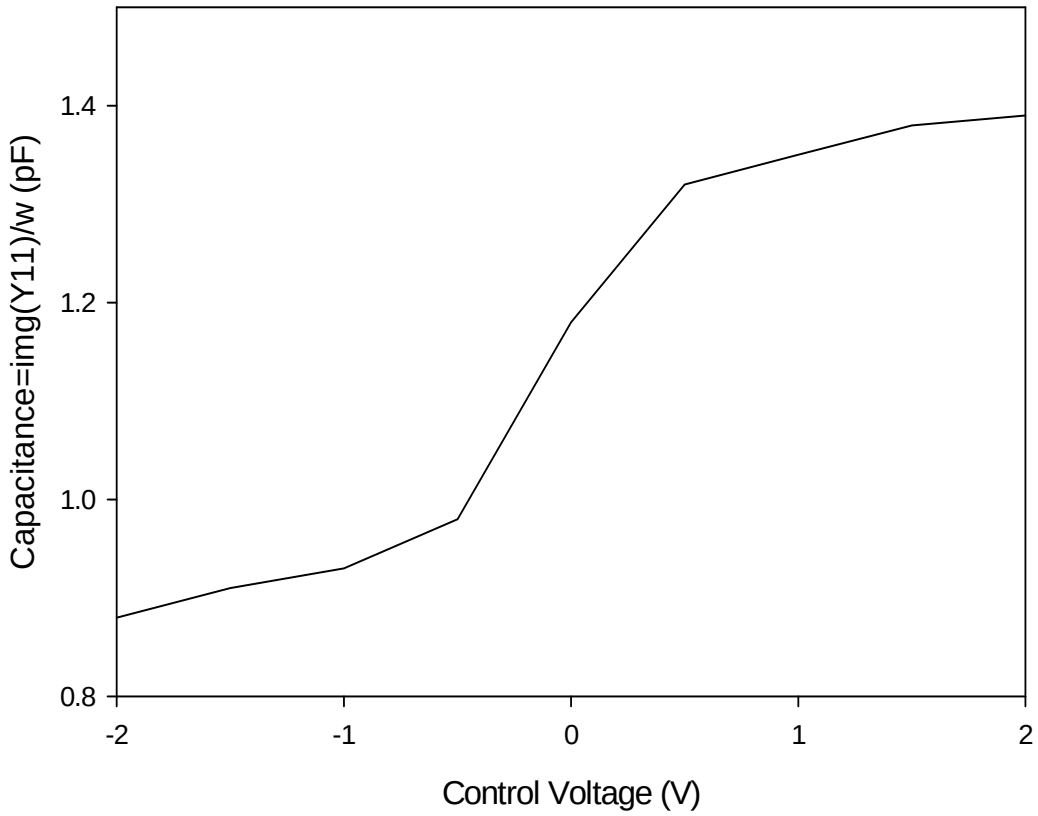




$$\frac{1}{C_T} = \frac{1}{C_{ox}} + \frac{1}{C_{dep}}$$

$$Q_C = \frac{1}{\omega R_S C_T}$$

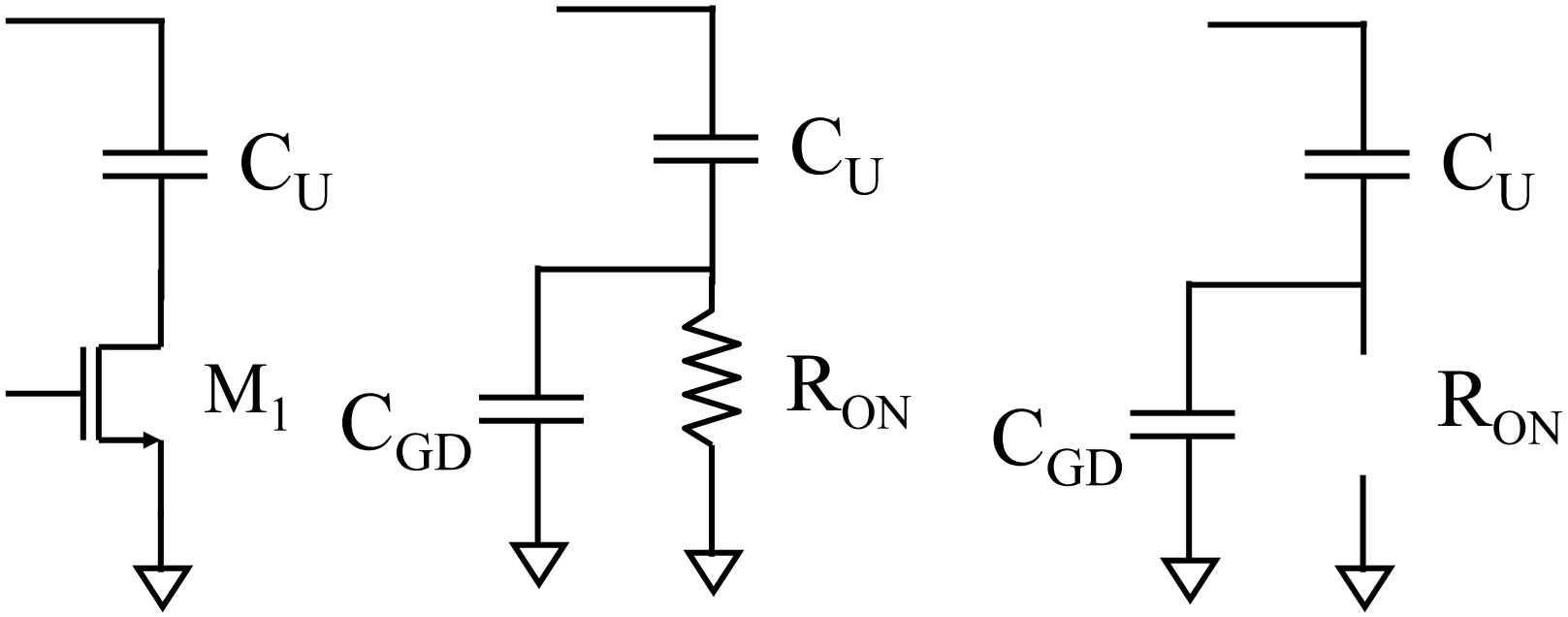
Accumulation-Mode Varactor



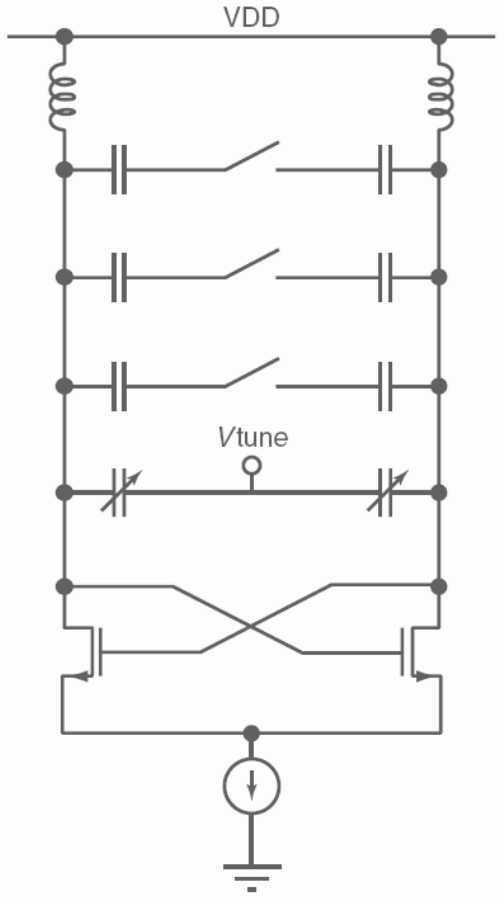
Accumulation-Mode Varactor

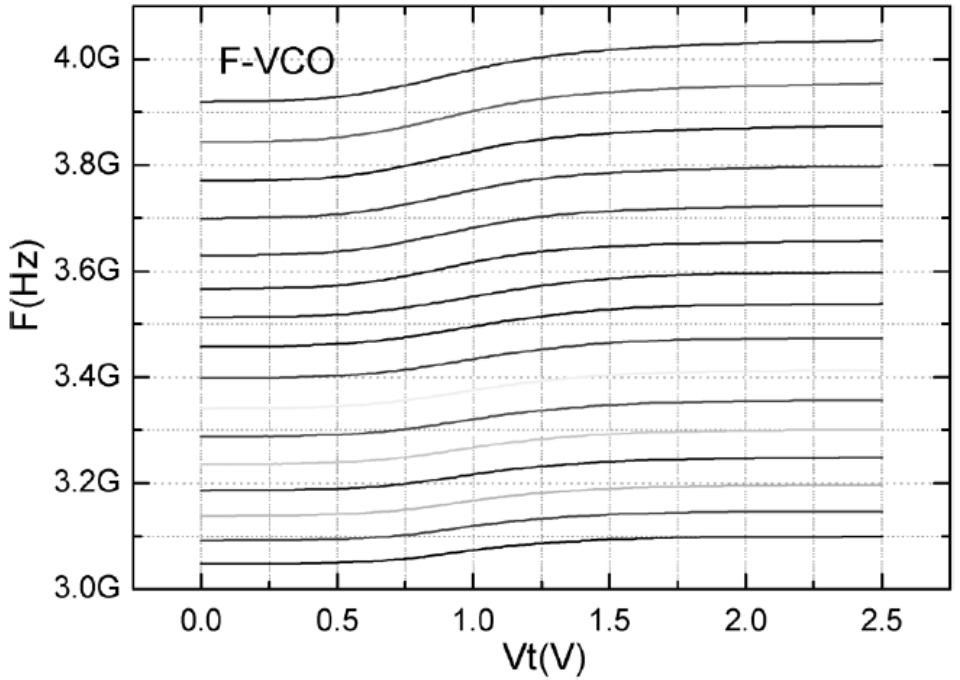
- Similar to NMOS with N-Well Instead of P-Substrate
- n+ Are Used to Minimize Parasitic p-n Junction Capacitance to Maximize Tuning
- For Gate Voltage Larger Than Flat-Band Voltage V_{FB} => Accumulate => $C_T = C_{ox}$
- For Smaller Gate Voltage, Depletion Capacitance C_{dep} Exists Between Oxide and N-Well => $1/C_T = 1/C_{ox} + 1/C_{dep}$
- Compared to p-n Junction Capacitance, Advantages of Accumulation-Mode Capacitance Include [Soorapanth]:
  - Better Average Q
  - Larger Tuning Capacitance

Switchable-Capacitance Array

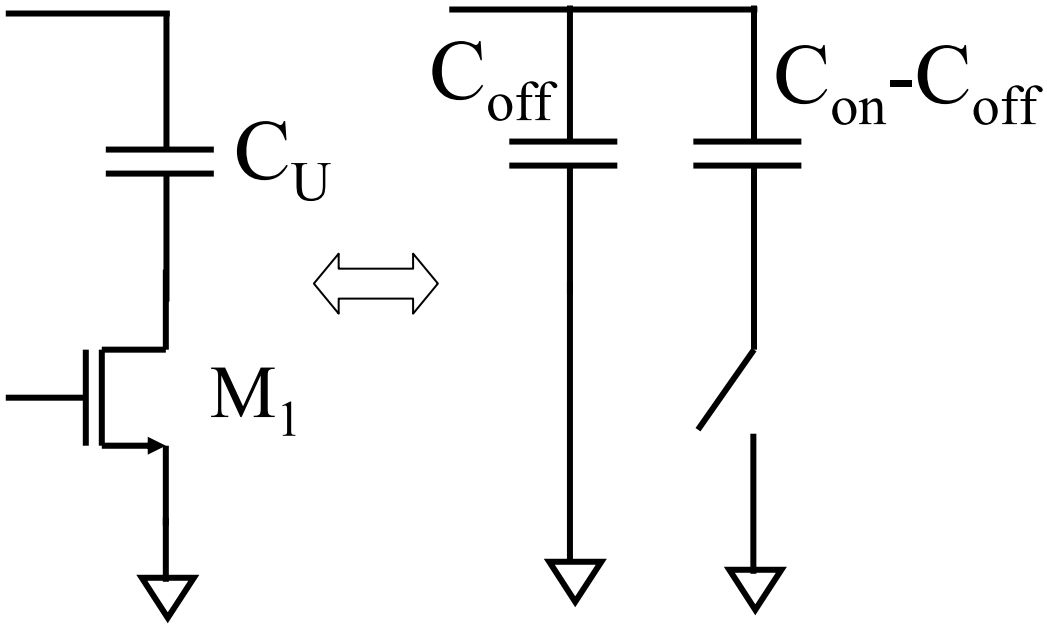


Larger Tuning Range





Switchable-Capacitance Array



$$C_{on} = C_u$$

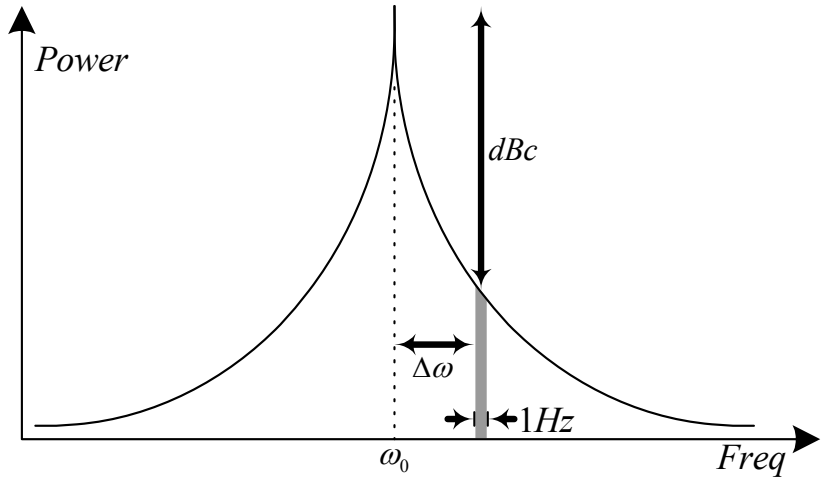
$$C_{off} = \frac{C_u C_{gd}}{C_u + C_{gd}}$$

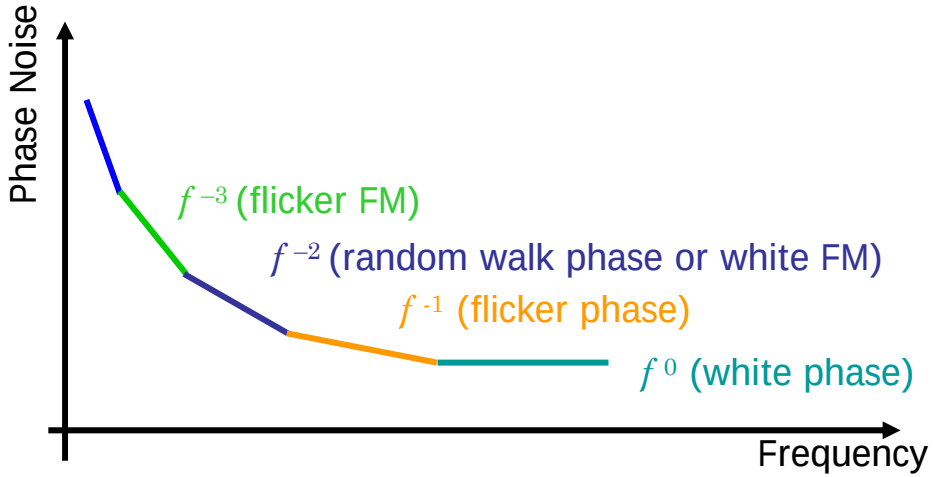
$$Q_C = \frac{1}{\omega R_{on} C_{on}}$$

Switchable-Capacitance Array

- Wide Tuning Range Can Be Achieved By Increasing Number of Bits in the Array
- Large Switch => Small Turn-On Resistance => High Q
- Large Switch => Large Parasitic Capacitance => Small Tuning Range and Limited Operating Frequency

Phase Noise Estimation



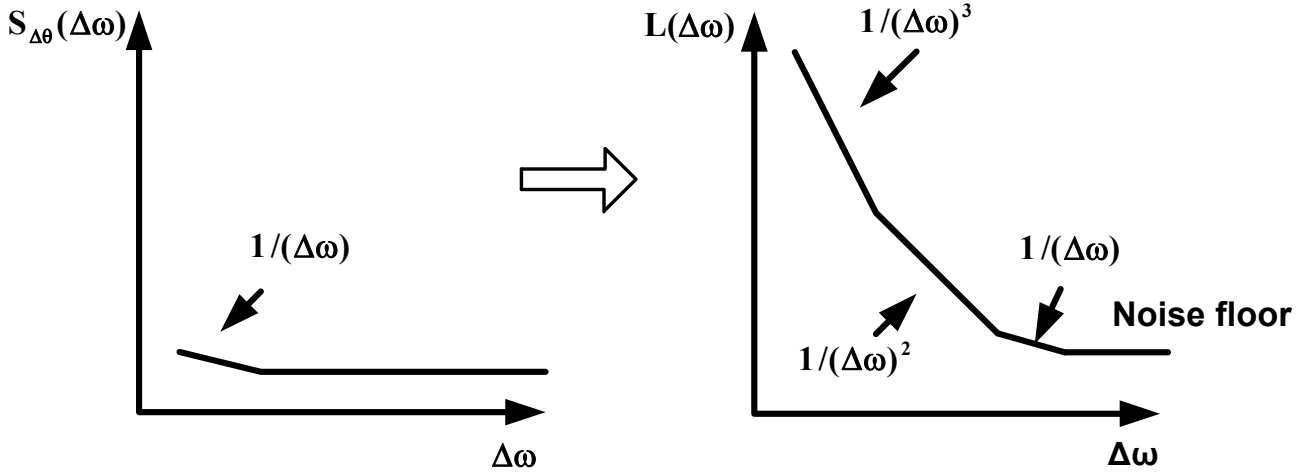


$$\mathcal{L}_{total}\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right]$$

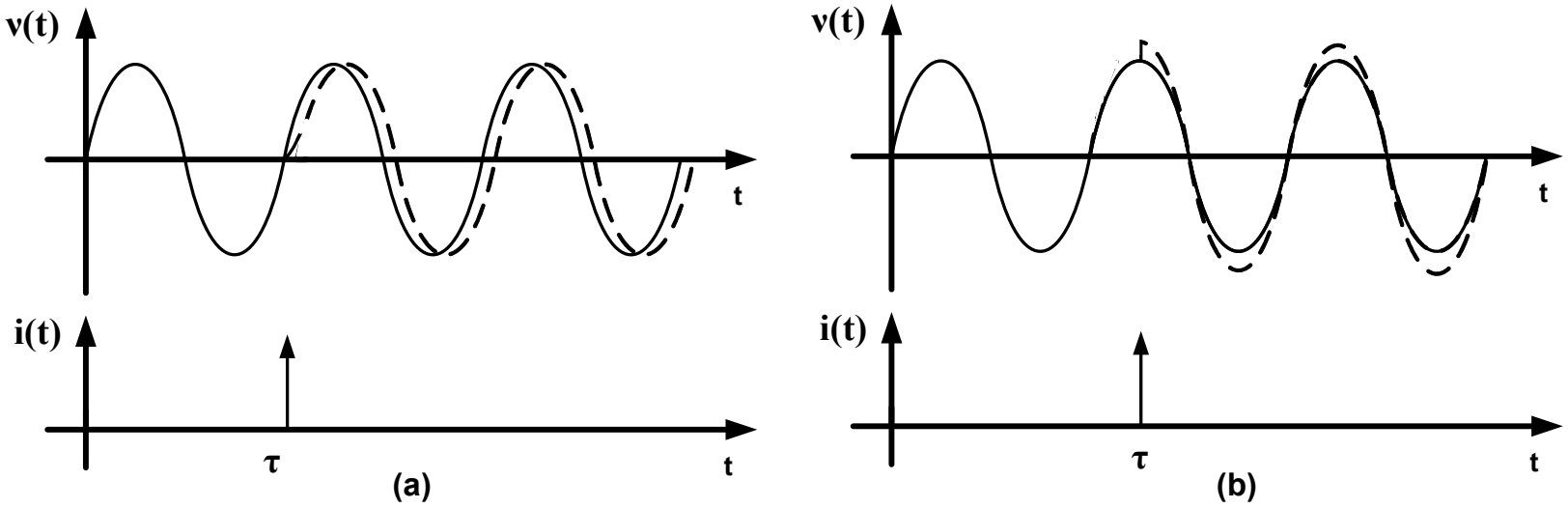
Phase Noise Estimation-Leeson's Model

$$L(\Delta\omega) = S_{\Delta\theta}(\Delta\omega)\left[1 + \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]$$

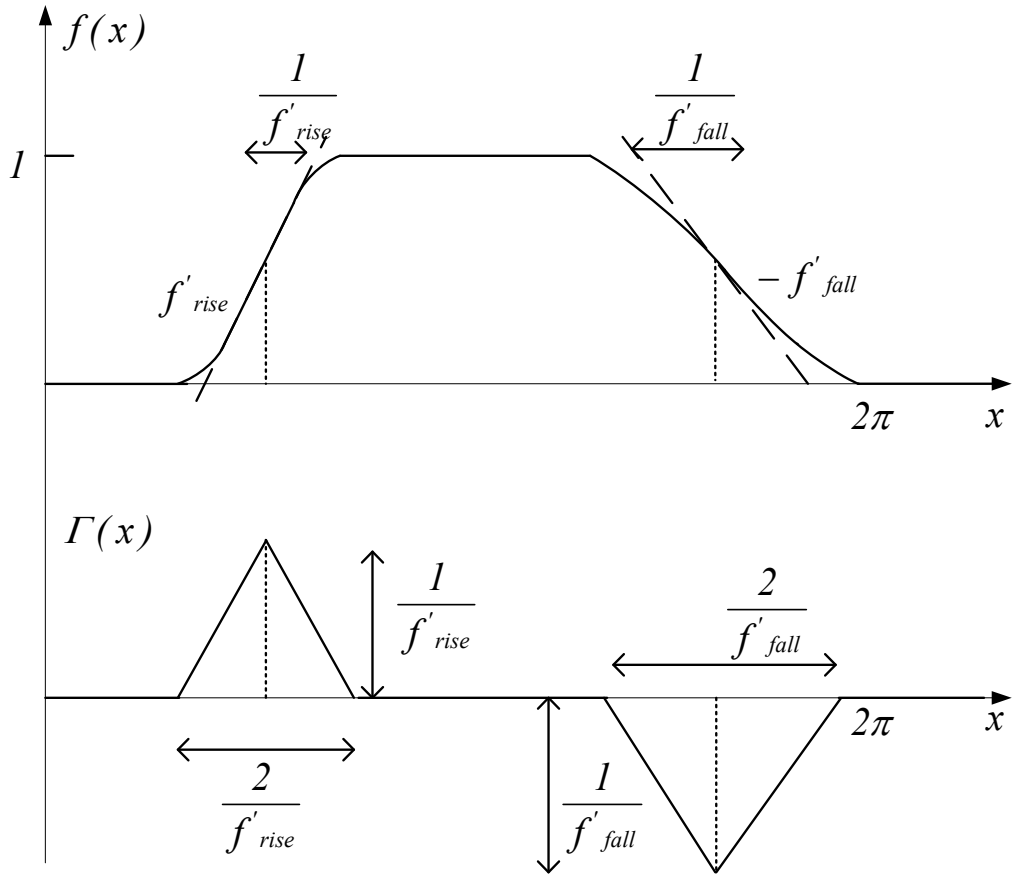
$$S_{\Delta\theta}(\Delta\omega) = \frac{\alpha}{\Delta\omega} + \frac{2FkT}{P_s}$$



Phase Noise – Hajimiri's Theory



Phase Noise – Hajimiri's Theory



Phase Noise – Hajimiri's Theory

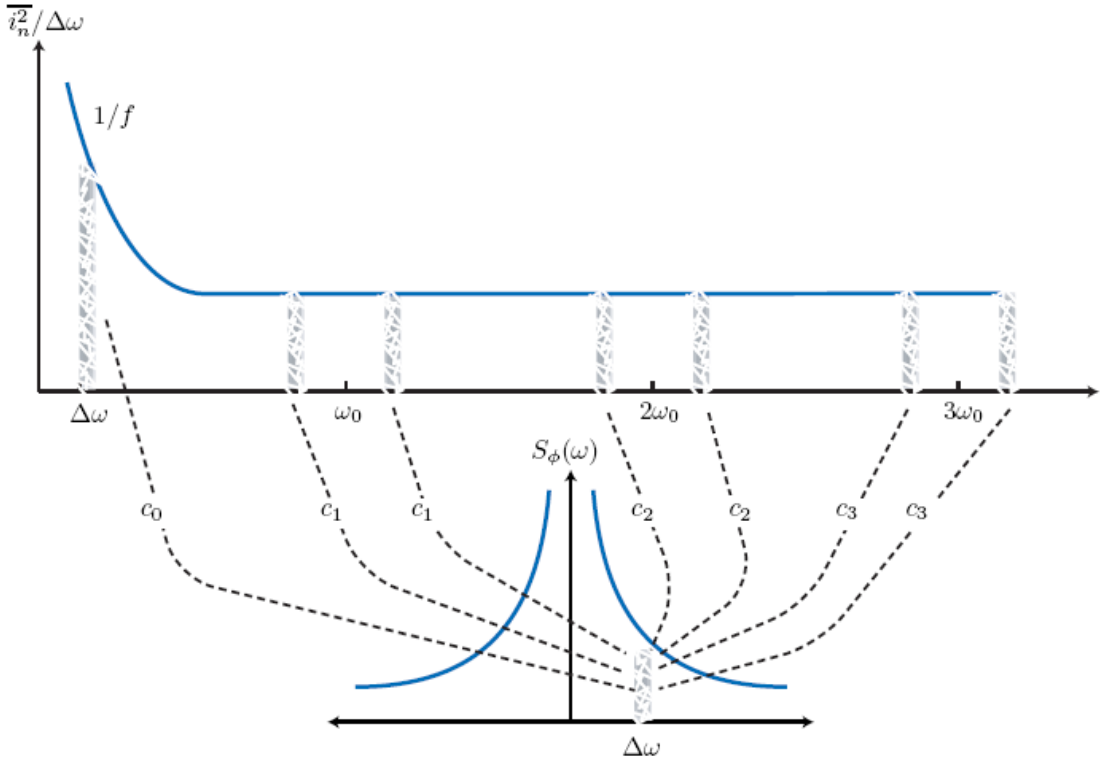
- Use Impulse Sensitivity Function (ISF) G(x) which is a Periodic Function of Phase Shift for A Unit Impulse Applied at Time t = x
- Phase Noise is Maximum when Noise Current Impulses are Injected at Zero-Crossing Point
- Phase Noise is Minimum when Noise Current Impulses are Injected at Output Peaks

Phase Noise – Hajimiri's Theory

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2(\Delta\omega)^2}$$

$$L(\Delta\omega) = \frac{c_0^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{8(\Delta\omega)^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}$$

Phase Noise in the VCO

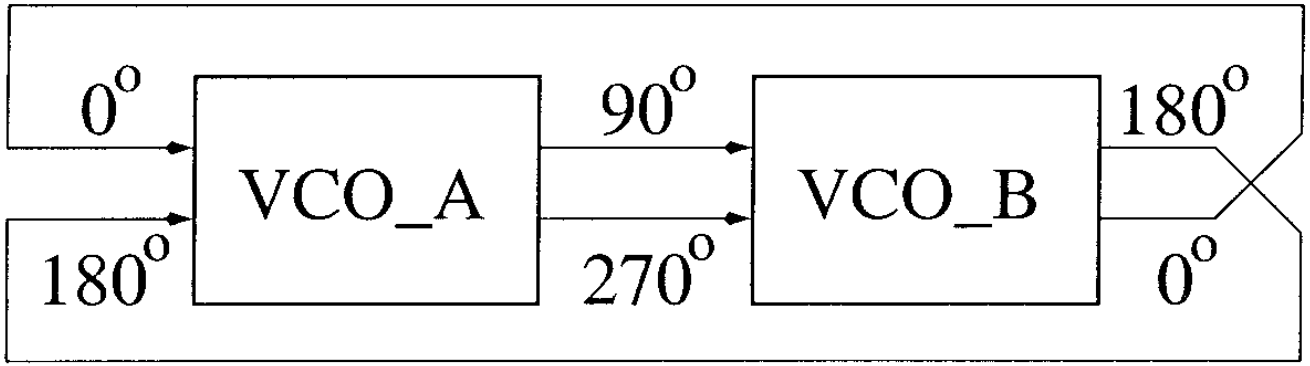


We see that all noise a distance ω around all the harmonics, including DC, contributes to the phase noise. DC 1/f noise contributes to the $1/f^3$ region.

Optimization of Phase Noise in the LC VCO

- Evaluate the optimization gate length of the active device
- Calculate minimize spectral density of each oscillator noise source by using the optimization gate length of the active device.
- Derive the impulse sensitivity function of each oscillator source after the transient simulation is done when a current noise is injected at the node of the oscillator circuit (Cadence SpectreRF).
- Combine above results to obtain for each oscillator noise source.
- Calculate Fourier Series Coefficient for each ISF
- Calculate the overall output phase noise using the results from above step.

Quadrature Phase Generator



- Divide-by-2
- Quadrature VCO
- Poly phase shifter (RC-CR network)