Sensitivity Approach to Statistical Signal Integrity Analysis of Coupled Interconnect Trees *

Zhigang Hao and Guoyong Shi
School of Microelectronics, Shanghai Jiao Tong University, Shanghai 200240, China
{haozhigang, shiguoyong}@ic.sjtu.edu.cn

***Abstract*— Capacitive and inductive coupling issues are hard to analyze in general; however, they are critical for signal integrity (SI) analysis in the contemporary integrated circuit technology. This paper presents a sensitivity based computation approach to coupled RLC trees for statistical signal integrity analysis. This technique is intended for use in SI-driven placement and routing.**

I. INTRODUCTION

In deep sub-micron interconnect design, signal integrity (SI) related problems greatly affect the design performance and reliability. Moreover, due to process variation, timing and SI effects are becoming statistical rather than deterministic. The existing approaches for signal integrity analysis can be divided into two categories. One is analytical model based [1], [2], [3], [4]. These models are simple and efficient but they are designed for special case analysis. Another kind is using model order reduction, which can be used in general for various cases. A key technique for model order reduction is the so-called *moment matching* [5], [6], which uses higher order moments to improve timing approximation and other dynamical characteristics. In addition, statistical model order reduction have been widely used for statistical modeling and timing analysis by many authors [7], [8] from different perspectives.

Moment-based signal timing metrics have also been studied by many publications [9], [10], [11]. For coupled RC circuits, simple metrics based on moments for crosstalk analysis are reported in [12], [13], [14]. However, for RLC circuits with strong inductance effects, there do not exist simple yet accurate metrics. Then, model order reduction becomes a good candidate for SI analysis.

Iterative tree traversal algorithms exist for moment computation of RLC trees [15], [16]. These iterative algorithms have been extended to deal with *capacitively* coupled RLC trees [17], but without considering *inductive* couplings. These recursive algorithms are good for numerical computations, but not for variational analysis that requires repeated computation of the same circuit structure.

Recently, a symbolic moment calculation mechanism is introduced in [18] and a symbolic moment calculator (SMC) has been implemented for interconnect trees considering both the *capacitive coupling* and *inductive coupling*. Alternative to the numerical calculation based model order reduction [5], [6], a symbolic model order reduction approach based on tree traversal, is proposed for signal integrity analysis in this paper.

Furthermore, a Direct Mapping algorithm based on sensitivity is presented, which is demonstrated to be accurate and efficient for statistical signal integrity analysis of strongly coupled interconnect trees.

The major contribution of this paper is the efficient and accurate sensitivity technique for statistical analysis of signal integrity effects of coupled interconnects, which can be used for SI-driven placement and routing in the future.

* This research was supported in part by Shanghai Pu Jiang Investigator Fund (Grant No. 07pj14053), the initiative research fund for overseas returnees from the Ministry of Education of China (2008), and by the National Natural Science Foundation of China, Grant No. 60876089.

The remainder of the paper is organized as follows. The background of symbolic moment calculator (SMC) for coupled interconnects is introduced in Section II. Symbolic model order reduction algorithm (SMOR) for tree structured circuits is proposed in Section III. In Section IV, the Direct Mapping algorithm is presented. Applications to statistical timing and signal integrity analysis are reported in Section V. A conclusion is drawn in Section VI.

II. BACKGROUND REVIEW

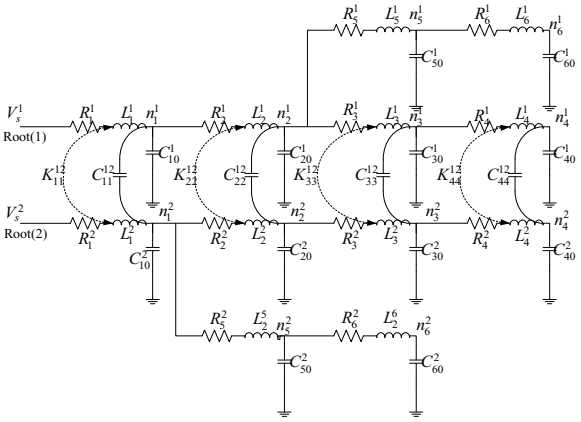

Fig. 1. Two RLC trees coupled.

An example of coupled RLC tree circuit is shown in Fig. 1. For moment computation, a coupling capacitor is modeled by two grouped current sources [17], while a pair of coupled inductors are modeled by two voltages sources [18]. The recursive moment computation algorithm with coupling is summarized below:

$$m_C^i(j,k) = \sum_{R_\ell^i \in P_\ell^i} R_\ell^i m_L^i(\ell,k) - \sum_{L_\ell^i \in P_\ell^i} L_\ell^i m_L^i(\ell,k-1) - \sum_{L_\ell^i \in P_\ell^i} M_{j,j'}^{i,i'} \sum_{L_{j'}^{i'} \in \mathbb{L}_\ell^i} m_L^{i'}(j',k-1); \quad (1)$$

$$m_L^i(j,k) = \sum_{n_j^i \in \mathbb{N}^i} C_j^i m_C^i(j,k-1) + \sum_{C_{j'}^{i'} \in \mathbb{C}_j^i} C_{j,j'}^{i,i'} \left[m_C^i(j,k-1) - m_C^{i'}(j',k-1) \right], \quad (2)$$

where $m_C^i(j,k)$ and $m_L^i(j,k)$ are the k^{th} order capacitor moment for $C_{j,0}^i$ and the k^{th} order inductor moment for L_j^i, respectively, $M_{j1,j2}^{i1,i2} = K_{j1,j2}^{i1,i2}\sqrt{L_{j1}^{i1} L_{j2}^{i2}}$ is the mutual inductance between inductors L_{j1}^{i1} and L_{j2}^{i2}, P_j^i is the path from $root(i)$ to node n_j^i in tree T^i, $\mathbb{C}_j^i$ is the set of coupling capacitors at node n_j^i, $\mathbb{L}_j^i$ is the set of inductors mutually coupled with L_j^i.

The recursive moment computation formulas in the form of (1) and (2) can be represented by a computation diagram, named the

Authorized licensed use limited to: Shanghai Jiao Tong University. Downloaded on October 6, 2009 at 12:21 from IEEE Xplore. Restrictions apply.

Moment Decision Diagram (MDD), in which the solid arrow stands for addition and the dashed arrow stands for multiplication. The example circuit shown in Fig. 1 is a coupled RLC tree with two input sources V_s^1 and V_s^2. The MDD for the given circuit is shown in Fig 2, where the nodes marked C's form a C-tree and the vertices marked R's form a binary decision diagram (BDD) R-tree with the only terminating $Zero$ vertex. The example circuit can be decoupled into two MDDs, each containing a C-tree and a R-tree. As is shown in Fig 2, two MDDs are linked with each other via the coupling capacitors and mutual inductors. For moment evaluation, the C-tree nodes store the inductor moments as the partial sum over the subtree rooted there, as seen from the equation (2), while the moments of any specific order are computed at the R-tree vertices using equation (1); and they are supplied recursively to the C-tree nodes for computing the next order moments. Thus, recursively all the k^{th} order moments of all nodes can be computed via MDDs traversal once the $(k-1)^{th}$ order moments have been obtained. The memory and time complexities are respectively $O(n)$ for a circuit with n nodes and $O(np)$ for computing up to the p^{th} order moment.

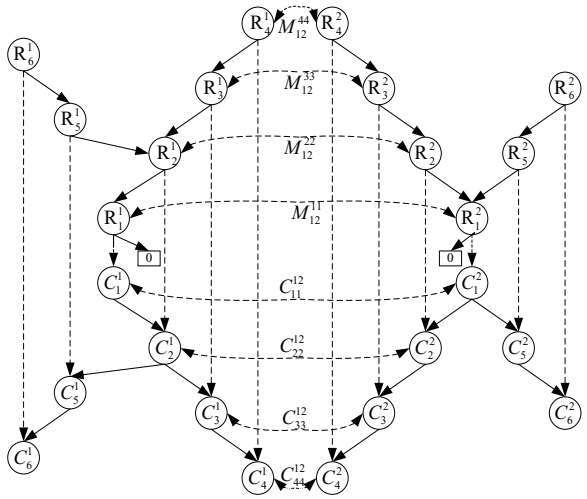

Fig. 2. Coupled moment decision diagram.

Once the MDDs have been constructed and stored in memory, moment computation turns out to be tree traversals according to algorithm (1) and (2). Thus moment recomputation can be made very efficient as circuit parameters change, and this makes MDD a very suitable data structure for moment recalculation under parameter variation.

III. SYMBOLIC MODEL ORDER REDUCTION

Tree structured RLC circuits can be modeled in the following state-space form

$$\widetilde{E}\frac{dx}{dt} + \widetilde{A}x = \widetilde{F}V_{in} \tag{3}$$

where

$$\widetilde{E} = \begin{bmatrix} C & 0 \\ 0 & L \end{bmatrix}, \widetilde{F} = -\begin{bmatrix} 0 & \cdots & 0 \\ e_1 & \cdots & e_N \end{bmatrix},$$

$$\widetilde{A} = \begin{bmatrix} 0 & A \\ -A^T & G^{-1} \end{bmatrix}, V_{in} = \begin{bmatrix} V_1 & \cdots & V_N \end{bmatrix}^T,$$

symmetry matrices C and L are capacitance and inductance stamping matrices including self and coupling capacitance, self and mutual inductance, respectively, $G = diag(G_1, G_2, \ldots, G_n)$ (where $G_i = R_i^{-1}$) is a diagonal matrix containing circuit resistor values, the first half of the unknown vector x contains the nodal voltages while the second half contains the branch currents. A is the incidence matrix of the circuit, while $\widetilde{F}$ and V_{in} represent the circuit source information in which e_k is the kth canonical vector. For more details on symbolic model order reduction (SMOR), see [19].

Moments, as coefficients of s^i in the expansion of $H(s) = \left(\widetilde{E}s + \widetilde{A}\right)^{-1}\widetilde{F}$, are

$$m^{(0)} = \widetilde{A}^{-1}\widetilde{F}, \quad m^{(1)} = \left(\widetilde{A}^{-1}\widetilde{E}\right)m^{(0)}, \quad \ldots.$$

In general, the moments are expressed by

$$\begin{bmatrix} m_C^{(k)} \\ m_L^{(k)} \end{bmatrix} = \begin{bmatrix} \widetilde{G}^{-1}Cm_C^{(k-1)} - \widetilde{L}^{-1}Cm_C^{(k-2)} \\ A^{-1}Cm_C^{(k-1)} \end{bmatrix} \tag{4}$$

where $\widetilde{L}^{-1} = A^{-T}LA^{-1}$.

Symbolic moments up to order q are used to form a Krylov subspace

$$K_q = \left\{m^{(0)},\ m^{(1)},\ \cdots,\ m^{(q-1)}\right\}$$

which will be used as a projection matrix $V = \left[V^{(c)T},\ V^{(\ell)T}\right]^{\mathrm{T}}$ for model order reduction after the $numerical$ Gram-Schmidt orthonormalization. And we denote $V^T = [w_1, w_2, \cdots, w_{2n}]$ in row vectors for use below. After projection, the reduced order model matrices are obtained by the following tree traversal algorithm, rather than direct matrix-matrix products.

$$\begin{aligned}
\hat{E} &= V^T\widetilde{E}V = V^{(c)T}CV^{(c)} + V^{(\ell)T}LV^{(\ell)} \\
&= \sum_{i=1}^{n} C_i w_i w_i^T + \sum_{i=1}^{n}\sum_{C_{ij}\in\mathbb{C}_i} C_{ij}\left(w_i w_i^T - w_i w_j^T - w_j w_i^T\right) \\
&+ \sum_{i=1}^{n} L_i w_{n+i} w_{n+i}^T + \sum_{i=1}^{n}\sum_{M_{ij}\in\mathbb{L}_i} M_{ij}\left(w_{n+i}w_{n+j}^T + w_{n+j}w_{n+i}^T\right) \\
\hat{A} &= V^T\widetilde{A}V = V^{(c)T}AV^{(\ell)} - \left[V^{(c)T}AV^{(\ell)}\right]^T + V^{(\ell)T}RV^{(\ell)} \\
&= \sum_{i=1}^{n}(w_i - w_{p(i)})w_{n+i}^T - \sum_{i=1}^{n} w_{n+i}(w_i^T - w_{p(i)}^T) \\
&+ \sum_{i=1}^{n} R_i w_{n+i} w_{n+i}^T, \\
\hat{F} &= V^T\widetilde{F} = -\begin{bmatrix} w_{n+in1} & \cdots & w_{n+inN} \end{bmatrix},
\end{aligned}$$

where $p(i)$ denotes the parent node index of node i with $w_{p(1)} = 0$, $\mathbb{C}_i$ is the set of coupling capacitors at node i and $\mathbb{L}_i$ is the set of inductors mutually coupled with L_i.

Because $\widetilde{A}$ is positive semi-definite and invertible, we have $\widetilde{A} > 0$. Also $\widetilde{E}$ is positive-definite. Therefore, the congruence transform does not change the positive-definiteness. Hence, the stability of a reduced order model is guaranteed. The case of RC tree-structured circuit is a special case of an RLC circuit by setting all L's to be zero.

IV. DIRECTLY MAPPED PDFS FOR STATISTICAL SIGNAL INTEGRITY ANALYSIS

In practice, one would like to know the peak noise and delay noise distribution of selected victim path under circuit parameter variation. Most methods proposed in literature use general Monte Carlo simulations [7] or accelerated Monte Carlo simulations, being interval-based [8] or first-order approximation based [14]. Until recently, the authors in [20] used the joint probability distribution function to analyze signal integrity effects statistically for high speed system packaging.

We use the similar PDF metrics following the work in [20]. Let X be a real random variable with the probability density function (PDF) $f_X(x)$. Let $y = g(x)$ be a first-order differentiable function of x. In Probability Theory, the PDF of the random variable Y satisfies

$$f_Y(y) = \sum_k \frac{f_X(x_k)}{|dg(x_k)/dx|} \tag{5}$$

Authorized licensed use limited to: Shanghai Jiao Tong University. Downloaded on October 6, 2009 at 12:21 from IEEE Xplore. Restrictions apply.

where x_k, $k = 1, 2, ...$, are all points satisfying $g(x_k) = y$. Similar identities exist for multi-variable functions [21].

The moments obtained using SMC in Section II can be used for model order reduction or direct moment metrics. For RC circuits, the work in [10] used two orders of moment for delay estimation while the authors of [12] and [13] used up to first three orders of moments for crosstalk noise analysis. For RLC circuits, moment based timing metrics are used in [9], [11]. In this paper, symbolic model order reduction based on tree traversing is used for signal integrity analysis for coupled RLC trees, from which the timing, signal integrity information can be obtained simultaneously. The sensitivity part in (5) is

$$\left.\frac{\partial g(x)}{\partial x}\right|_{x=x_k} = \frac{g(x_k + \Delta x) - g(x_k)}{\Delta x}, \tag{6}$$

which can be computed by running SMC and SMOR twice.

Direct Mapping Algorithm

Step 1.Compute the sensitivity of the measuring criteria (signal delay, peak noise, delay noise, etc) with respect to circuit parameters $dg(x_k)/dx$ in (5) using repeated SMC and SMOR calculation.

Step 2.Compute the joint probability density function of measuring criterion $f_Y(y)$ in (5) using probability density function of circuit parameters.

Step 3.Run Step 1 and Step 2 repeatedly over a set of samples to reconstruct the joint PDF of the measuring criteria until an adequate distribution is obtained.

Once the joint PDF of signal integrity measures has been constructed with adequate sample points, the statistical variations of the circuit parameters are reflected by the distribution of SI measures. Design yield and performance can be estimated from the calculated PDFs.

V. Experimental Results

In this section, two coupled interconnect tree designs (shown in Table II) are used to demonstrate the application of our algorithm to statistical interconnect analysis. We implemented our SMC algorithm in C++ and tested on an Althon64 4400+ CPU with 2GB memory running a Ubuntu 8.10 operating system. The performance was compared to HSPICE version 2005.03 running on the same machine. The input to the driver is a $1V$ step voltage source with source resistance 50Ω. The per-unit-length (PUL) parameters are $r = 5.36m\Omega$, $\ell = 0.61nH$, $c = 0.14pF$, $cc = 0.0155pF$, $k = 0.9$.

As the first part of experiment, we observed the effect of reduced model order on the accuracy of symbolic model order reduction compared with HSPICE. The 50% delay of step response was used for the accuracy measurement. The average error of all nodes of Design #1 and #2 compared with HSPICE on selecting orders is shown in Table I. We found that for the case of coupling RC circuit, order 4 is sufficient for almost all cases. While for RLC circuits with strongly coupled inductors, higher orders, say, 6, 8 or more are needed to get satisfactory accuracy. Shown in Fig. 3 is the selected step response of two far-end nodes of both the aggressor line and the victim line of Design #1.

Compared to the average error of 32.04% stated in [11] using the moments up to 6th order for RLC circuits and the average error of 1.76% using the moments up to the 3rd order for RC circuits, our SMOR simulator clearly outperforms in accuracy for both RLC and RC tree circuits.

We also tested our simulator for a few extremely large circuits. For example, for a tree circuit with one million R/L/C elements, the total time for generating symbolic moment up to 6th order and getting the reduced order model for all nodes took 102 seconds and 87MB memory. As far as memory allows, our simulator using SMC and SMOR can possibly deal with the scale of ten million elements or more (but the netlist parsing time would be long).

TABLE I
Reduced orders versus delay accuracy.

Design	Order	mean-error(%)	max-error(%)	std-error(%)
#1	6	9.43	16.36	8.32
	8	7.29	13.18	5.66
	10	4.52	8.29	2.95
#2	2	3.35	6.26	3.33
	3	2.29	2.38	1.66
	4	0.82	1.29	0.95

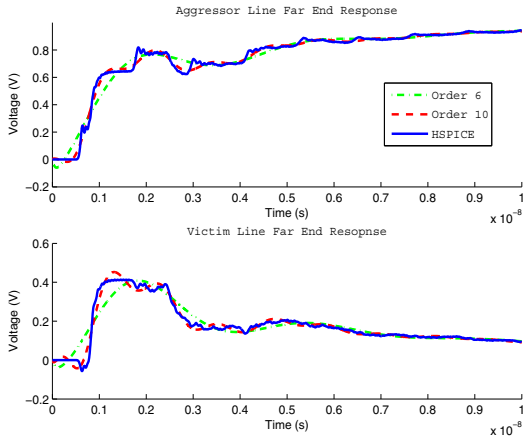

Fig. 3. Step response of two far-end nodes from Design #1.

In the second part of experiment we would like to inspect the statistical analysis accuracy of the Direct Mapping Algorithm. Similar to the work in [3], the victim line peak noise and delay noise are used for measuring. Shown in Table II are the collected test results for the two design cases. For Design #1 the per-unit-length inductance value is assumed to be the varying parameter for delay noise measurement while the source resistance value is assumed to be the varying parameter for peak noise measurement. For Design #2 the source resistance value is assumed to be the varying parameter for both measurements. All varying parameters are assumed to be Gaussian variables with 30% variation corresponding to 3σ. For each design case, 3 nodes, one near-end node, one mid-end node and one far-end node, were selected in the victim line for measurement. We used 5000 Monte Carlo samples for both the symbolic model order reduction and HSPICE and 40 sample points for Direct Mapping algorithm.

As can be seen from the table, our SMC simulator using SMOR was accurate in the measurement except for a few near-end nodes. In fact, larger errors commonly occurred at the near-end nodes, which is also common to other moment based metrics such as the Elmore delay and D2M [10], etc. The reason is simple; signals at the near-ends transit faster than at the far-ends, hence higher-order models are necessary to catch up the fast modes. The Direct Mapping using SMOR achieved the accuracy equal to the Monte Carlo SMOR, but with great speed-ups compared to HSPICE as shown in Table II. Shown in Fig. 4 and Fig. 5 are two measured distribution comparison results between HSPICE Monte Carlo and Direct Mapping approach.

VI. Conclusion

A sensitivity based Direct Mapping approach to statistical analysis of signal integrity effects of coupled interconnect trees is proposed. It

Authorized licensed use limited to: Shanghai Jiao Tong University. Downloaded on October 6, 2009 at 12:21 from IEEE Xplore. Restrictions apply.

TABLE II

TIMING AND SIGNAL INTEGRITY RELATED MEASURES BETWEEN HSPICE MONTE CARLO, DIRECT MAPPING AND SMOR MONTE CARLO

Analysis Type	Variation	Node Type	HSPICE		Direct Mapping		Speed Up	SMOR		Speed Up
			mean	std	mean	std		mean	std	
Design #1 Coupled R 600, L 600, C 600 Reduced Order = 10										
Delay Noise	30%	Near-end	227.6(ps)	9.7(ps)	7.5%	4.3%	2580	7.8%	4.1%	47
		Mid-end	555.2(ps)	25.2(ps)	5.2%	3.3%		6.4%	4.1%	
		Far-end	865.4(ps)	41.1(ps)	2.1%	1.5%		1.4%	1.2%	
Peak Noise	30%	Near-end	421.9(mV)	9.1(mV)	6.8%	3.8%	2532	6.6%	4.9%	46
		Mid-end	441.9(mV)	10.3(mV)	3.1%	3.1%		4.1%	2.8%	
		Far-end	424.6(mV)	10.4(mV)	1.5%	1.7%		1.1%	1.9%	
Design #2 coupled R 1000, C 1000 Reduced Order = 4										
Delay Noise	30%	Near-end	1084.2(ps)	133.1(ps)	0.2%	1.5%	1542	0.2%	1.8%	28
		Mid-end	1053.7(ps)	127.5(ps)	0.2%	1.2%		0.1%	1.3%	
		Far-end	1046.9(ps)	126.2(ps)	0.1%	1.1%		0.1%	1.0%	
Peak Noise	30%	Near-end	35.8(mV)	3.2(mV)	0.3%	1.6%	1579	0.1%	1.9%	28
		Mid-end	36.6(mV)	3.3(mV)	0.2%	1.0%		0.1%	1.2%	
		Far-end	36.7(mV)	3.3(mV)	0.1%	0.9%		0.1%	0.8%	

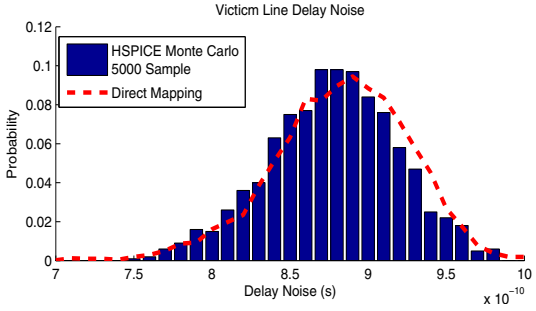

Fig. 4. Victim line far-end node delay noise distribution of design #1.

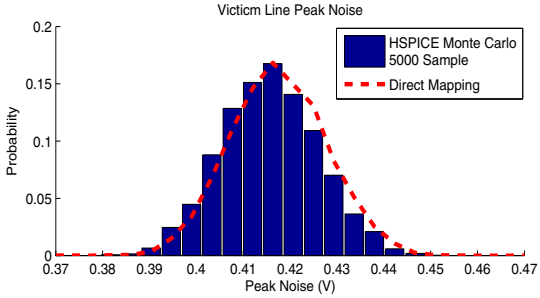

Fig. 5. Victim line far-end node peak noise distribution of design #1.

has been demonstrated that the proposed algorithm can perform accurately yet efficiently statistical timing and signal integrity analysis for large-scale interconnect trees. Future work includes application of our statistical simulator to industry scale routing, clock tree synthesis and crosstalk analysis.

REFERENCES

[1] L. Yin and L. He, "An efficient analytical model of coupled on-chip RLC interconnects," in *Proc. Int. Asia South-Pacific Design Automation Conference*, 2001, pp. 385–390.

[2] J. Zhang and E. G. Friedman, "Decoupling technique and crosstalk analysis for coupled RLC interconnects," in *Proc. Int. Symposium on Circuits and Systems*, 2004, pp. 521–524.

[3] K. Agarwal, D. Sylvester, and D. Blaauw, "Modeling and analysis of crosstalk noise and coupled RLC interconnects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 5, pp. 892–901, May 2006.

[4] T. Kim and Y. Eo, "Analytical CAD models for the signal transients and crosstalk noise of inductance-effect-prominent multicoupled RLC interconnect lines," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 7, pp. 1214–1227, 2008.

[5] L. Pillage and R. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design*, vol. 9, pp. 352–366, April 1990.

[6] A. Odabasioglu, M. Celik, and L. T. Pileggi, "PRIMA: Passive reduced-order interconnect macromodeling algorithm," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, no. 8, pp. 645–654, August 1998.

[7] X. Li, P. Li, and L. Pileggi, "Parameterized interconnect order reduction with explicit-and-implicit multi-parameter moment matching for inter/intra-die variations," in *Proc. Int. Conf. Computer-Aided Design*, Nov. 2005, pp. 806–812.

[8] J. D. Ma and R. A. Rutenbar, "Fast interval-valued statistical modeling of interconnect and effective capacitance," *IEEE Trans. on Computer-Aided Design*, vol. 25, no. 4, pp. 710–724, April 2006.

[9] A. B. Kahng and S. Muddu, "An analytical delay model for RLC interconnects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems* , vol. 16, no. 12, pp. 1507–1514, 1997.

[10] C. J. Alpert, A. Devgan, and C. Kashyap, "A two moment RC delay metric for performance optimization," in *Proc. International Symposium on Physical Design(ISPD)*, San Diego, CA, 2000, pp. 73–78.

[11] Y. I. Ismail and C. S. Amin, "Computation of signal-threshold crossing times directly from higher order moments," *IEEE Trans. on Computer-Aided Design*, vol. 23, no. 8, pp. 1264–1276, Aug. 2004.

[12] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects," in *Proc. Int. Conf. Computer-Aided Design*, Nov 1997, pp. 147–153.

[13] L. Chen and M. Marek-Sadowska, "Closed-form crosstalk noise metrics for physical design applications," in *Proc. Design Automation and Test Eur. Conf.*, 2002, pp. 812–819.

[14] K. Agarwal, M. Agarwal, D. Sylvester and D. Blaauw, "Statistical interconnect metrics for physical-design optimization," *IEEE Trans. on Computer-Aided Design*, vol. 25, no. 7, pp. 1273–1288, July 2006.

[15] C. L. Ratzlaff and L. T. Pillage, "RICE: Rapid interconnect circuit evaluation using AWE," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 13, no. 6, pp. 763–776, June 1994.

[16] Q. Yu and E. S. Kuh, "Exact moment matching model of transmission lines and application to interconnect delay estimation," *IEEE Trans. on Very Large Scale Integration Systems*, vol. 3, no. 2, pp. 311–322, June 1995.

[17] Q. Yu and E. S. Kuh, "Moment computation of lumped and distributed coupled RC trees with application to delay and crosstalk estimation," *Proceedings of the IEEE*, vol. 89, no. 5, pp. 772–788, May 2001.

[18] A. Liu, *A Symbolic Approach to the Signal Integrity of Multi-coupledd RLC Tree Circuits with Application*. Master Thesis, School of Microelectronics, Shanghai Jiao Tong University, 2009.

[19] G. Shi, B. Hu, and C.-J. R. Shi, "On symbolic model order reduction," *IEEE Trans. on Computer-Aided Design*, vol. 25, no. 7, pp. 1257–1272, July, 2006.

[20] E. Matoglu, N. Pham, D.N. de Araujo, M. Cases and M.Swaminathan, "Statistical signal integrity analysis and diagnosis methodology for high-speed systems," *IEEE Trans. on Advanced Packaging* , vol. 27, no. 4, pp. 611-629, Nov. 2004

[21] A. Papoulis, *Probability, Random Variables, and Stochastic Processes*. Boston, MA: WCB/McGraw-Hill, 1991

Authorized licensed use limited to: Shanghai Jiao Tong University. Downloaded on October 6, 2009 at 12:21 from IEEE Xplore. Restrictions apply.