A Design Platform for Analog Device Size Sensitivity Analysis and Visualization

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***Abstract*—A symbolic calculation method for the sensitivity of frequency response to semiconductor device sizes is addressed for application in analog integrated circuit design. The transistor-size-based ac-sensitivity can be used for sizing devices and understanding the circuit behavior. Examples are provided to demonstrate that a design platform supported by symbolic ac-sensitivity and visualization can be a helpful tool for computer-aided design of analog integrated circuit.**

***Index Terms*—ac-sensitivity, analog circuit design, binary decision diagram (BDD), device sizing, pole-zero analysis, symbolic simulation.**

I. Introduction

Symbolic circuit simulation is now receiving renewed research interest after the proposal of a new computation paradigm based on Binary Decision Diagram (BDD) around 2000 [1]. The BDD-based computation methodology can extend the capacity of a symbolic simulator to handle op-amp circuits containing over 20 transistors, and more if an advanced hierarchical implementation is adopted [2]. Before the new paradigm was proposed, exact symbolic ac analysis was only able to analyze circuits of size about ten transistors [3], [4], which was inadequate for practical use.

Typically, design of an analog integrated circuit involves many metrics that conflict to each other. A SPICE simulation tool can do accurate circuit analysis, but is unable to meet the designer's desire for design space exploration, such as to quickly identify the critical devices for performance optimization and sizing. Those analog synthesis tools proposed about twenty years ago ([5], [6], among others) attempted to use a search engine for optimization, but were not successful due to the blindness involved in search. While such methodologies are becoming obsolete, it seems that no significant innovative analog synthesis methodologies have been proposed recently in the literature. In the authors' opinion, analog circuit optimization largely relies on the basic understanding of the analytical interrelations underlying the device models, device sizes, and the design metrics. Such analytical relations so far have been mostly hand-handled by experienced analog designers in their design practice. A symbolic ac analysis tool is probably the only informative and efficient tool that can potentially handle such analytical interrelations with a certain level of automation.

One of the challenges faced by analog designers is that device sizing cannot be fully or partly automated, because device sizing is an involved practice that requires many years of design experience. If a design tool can in one way or another help the designer understand or even *visualize* which device has a stronger or weaker influence on the ac performance, it certainly would be a more informative design guide than any popular SPICE simulator.

This paper presents an analog design platform which utilizes a symbolic technique for the computation of ac-sensitivity with respect to device sizes. The previously published work as the foundation of this research includes [7] and [8], where a topological symbolic analysis algorithm incorporating BDD was proposed, and [9], where the ac-sensitivity to small-signal parameters was addressed. This work extends the previous work to investigate the ac-sensitivity to device sizes and provides a graphical visualization aid for visual assessment of the circuit pole-zero characteristics.

II. AC-Sensitivity to Device Size

Let $H(s)$ be the transfer function of a circuit network. The *ac-sensitivity* is defined to be the relative variation of $H(s)$ with respect to (w.r.t.) the variation of a circuit parameter, say p, which is typically written in a normalized form [10],

$$\mathrm{Sens}(H(s),p)=\frac{\partial \ln H(s)}{\partial \ln p}=\frac{p}{H(s)}\frac{\partial H(s)}{\partial p}. \qquad (1)$$

We are interested in deriving a symbolic expression for $\mathrm{Sens}(H(s),p)$ so that its plots can be visualized and manipulated interactively by altering the circuit parameter p. Here, the parameter can either be a device small-signal parameter or geometrical measures (*width* and/or *length*) of a semiconductor device. Since it is feasible to derive symbolic expressions for $H(s)$ in the ac-domain, it is thus possible to address the symbolic ac-sensitivity computation of $\mathrm{Sens}(H(s),p)$.

A computation method for the ac-sensitivity to one small-signal parameter was discussed in [9], where a graph-pair reduction scheme for symbolic construction of $H(s)$ in the form of a BDD, called *Graph-Pair Decision Diagram (GPDD)*, was applied for such a purpose. Because an $H(s)$ expressed in a BDD is naturally in the Sum-Of-Product (SOP) form, with the circuit parameters being the symbols in the SOP expression directly, taking derivative w.r.t. a circuit parameter in BDD is a trivial task and can be implemented easily.

The small-signal parameters of a MOSFET device are dependent on the fabrication process parameters, the device sizes (width W and length L), and the biasing condition at the operating point. Assuming the devices are in certain operating

This research was supported by the National Natural Science Foundation of China (Grant No. 60876089).

978-1-4244-7456-4/10/$26.00 ©2010 IEEE

region, the sensitivity of the small-signal parameters to the device sizes can be computed.

For example, the parameters given in the small-signal MOSFET model (Fig. 1) are determined by the following equations in the saturation region:

$$G_m = \sqrt{2k'\frac{W}{L}I_D}, \tag{2a}$$

$$R_{ds} = \frac{1}{\lambda I_D}, \tag{2b}$$

$$G_{mb} = \frac{\gamma G_m}{2\sqrt{2\phi + V_{sb}}}, \tag{2c}$$

$$C_{sb} = C_{db} = C_j L_s W + C_{jsw}(2L_s + W), \tag{2d}$$

$$C_{gs} = \frac{2}{3}C_{ox}WL + C_oW, \tag{2e}$$

$$C_{gd} = C_oW, \tag{2f}$$

where the meanings of the parameters are available in the textbook [11]. Then it is easy to compute the quantities such as $\mathrm{Sens}(G_m, W) = 0.5$, etc. Yang et al. [12], [13] addressed the device-size sensitivity in a data structure called *Element-Coefficient Diagram* (ECD) and used the computed sensitivity for automatic device sizing.

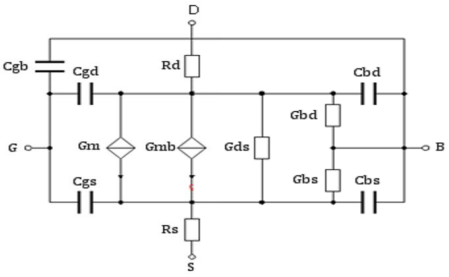


Fig. 1: MOSFET small signal model.

Suppose a set of small-signal parameters $\{p_k^{(i)} : i = 1, \cdots, m\}$ depend on the kth transistor width W_k. Then, the sensitivity of $H(s)$ w.r.t. W_k, $\mathrm{Sens}(H(s), W_k)$, can be computed by the following formula

$$\mathrm{Sens}(H(s), W_k) = \sum_{i=1}^{m} \mathrm{Sens}(H(s), p_k^{(i)}) \cdot \mathrm{Sens}(p_k^{(i)}, W_k), \tag{3}$$

where $\mathrm{Sens}(H(s), p_k^{(i)})$ can be computed from a symbolic expression of $H(s)$ in terms of the small-signal parameters $p_k^{(i)}$, which is compactly represented by a BDD [8], while $\mathrm{Sens}(p_k^{(i)}, W_k)$ can be computed from the small-signal device model as given in (2). For simplicity, we assume that the small variation of W_k only affects the small signal parameters of the kth MOSFET, which might not always hold strictly.

With a BDD representation of $H(s)$, it is feasible to compute the sensitivity of $H(s)$ with respect to either one parameter or multiple parameters. Since the representation of $H(s)$ is in SOP form, the computation of the derivative $\partial \ln H(s)/\partial \ln p$ is fairly simple. For example, let $H(s) = N(s)/D(s)$, where $N(s)$ and $D(s)$ are both SOP polynomials. Then, $\mathrm{Sens}(H(s), p) = \mathrm{Sens}(N(s), p) - \mathrm{Sens}(D(s), p)$. Assume $N(s) = apb + bpc + def$, where a, p, and b, etc. are symbols. Then

$$\mathrm{Sens}(N(s), p) = \frac{p}{N(s)}\frac{\partial N(s)}{\partial p} = \frac{apb + bpc}{N(s)} = \frac{N_p(s)}{N(s)},$$

where $N_p(s)$ contains the SOP terms of $N(s)$ involving the parameter p. The same treatment applies to the SOP expression $D(s)$. *Removing those product terms not involving a parameter* is an easy operation on a BDD, as explained in [8]. Let $D_p(s)$ be the product terms of $D(s)$ involving parameter p. We have

$$\begin{aligned} \mathrm{Sens}(H(s), p) &= \mathrm{Sens}(N(s), p) - \mathrm{Sens}(D(s), p) \\ &= \frac{N_p(s)}{N(s)} - \frac{D_p(s)}{D(s)}. \end{aligned} \tag{4}$$

We should point out that such sensitivity operation on a determinant decision diagram (DDD) [1] is not as straightforward as stated here. Therefore, we propose to compute the ac-sensitivity by *GPDD* [8].

The following algorithm summarizes the ac-sensitivity computation over an SOP represented by a BDD:

AC-Sensitivity Computation Algorithm

(*i*) Select a set of transistors for sensitivity analysis. Establish the association between the device small-signal parameters and the device sizes according to the operating regions.

(*ii*) Find the device sensitivity coefficients $\mathrm{Sens}(p_k^{(i)}, W_k)$, which are independent on the frequency point s_k.

(*iii*) For $i = 1, \cdots, m$, compute $\mathrm{Sens}(H(s), p_k^{(i)})$ using the BDD-based computation method given in equation (4).

(*iv*) Evaluate the BDD once at the frequency point s_k until all the frequency points are evaluated.

(*v*) Repeat the above steps until all the requested devices have been processed.

III. The SPADE Platform and Design Case Studies

The symbolic ac-sensitivity can be integrated in a graphical visualization platform, named *SPADE* (*A Simulation Platform for Analog Design Exploration*). This platform consists of a schematic editor (or a netlist reader), a symbolic simulator *GRASS* (*Graph Reduction Analog Symbolic Simulator*) [8], and a graphical user interface (GUI) for displaying the sensitivity plots and sizing the semiconductor devices. Other graphical displaying functionalities for ac response exploration also can be integrated. The purpose of the SPADE GUI is to provide the designer with an interactive interface to the symbolic engine running in the simulator core. The results of frequency response variation and sensitivity variation are displayed instantly as certain circuit parameters are changed manually via the interface. Currently the commercial simulator HSPICE is used for obtaining the numerical dc operating points in the process of sizing. In the future, a dedicated in-house SPICE simulator can be integrated to SPADE.

Next, two amplifier circuits are used to demonstrate the application of the sizing-oriented ac-sensitivity analysis. We shall see that the ac-sensitivity plots can reveal the pole-zero locations and which devices are more relevant to the poles and zeros. Such valuable information involved in the ac-sensitivity plots was not studied in [12], [13].

A. Design Case 1: A two-stage op-amp

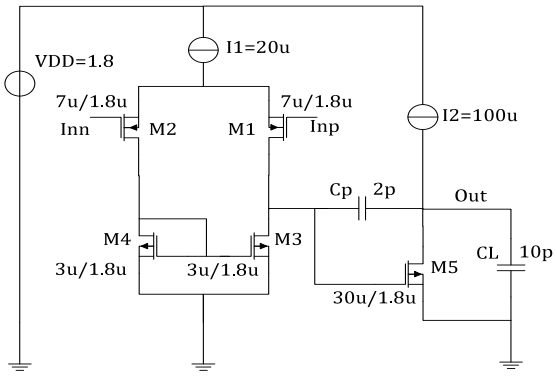


Fig. 2: A differential op-amp circuit containing five transistors.

The first example shown in Fig. 2 is a single-output two-stage differential amplifier containing five MOS transistors [11]. All transistors were sized to saturation manually first. Both the positive and negative input ports were biased at $0.6V$. A $1.0V$ ac source was connected to the positive input while the negative input was grounded. The dc operating point simulation used a $0.18\mu m$ technology library.

The design was targeted at the following specifications:
(1) Unity-gain frequency $f_t > 7.5MHz$, and
(2) dc gain $A_v > 100dB$.

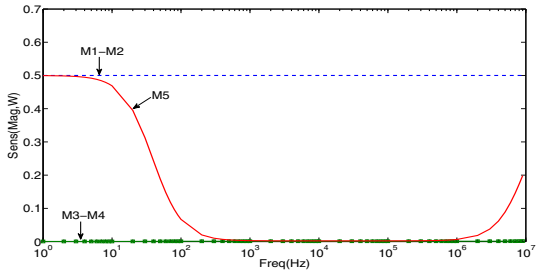
With the pair of M1-M2 sized to $W/L = 7\mu/1.8\mu$, the dc operating point was simulated by HSPICE to get the small-signal parameter values. They were used by the symbolic simulator GRASS to get the nominal frequency response after the BDD construction. The nominal ac response obtained by symbolic analysis was observed to *match accurately* that of HSPICE.

The initially sized ac response had a dc-gain close to 100dB, but the unity-gain frequency f_t was about $3.6MHz$, too lower than the required $7.5MHz$. At this moment we would like to know which devices to resize.

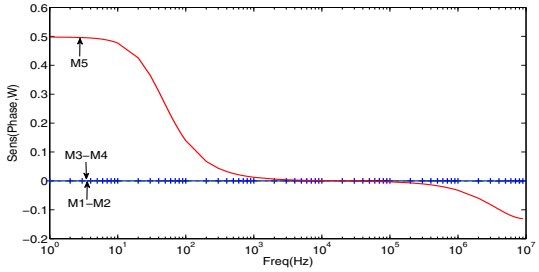
In practice, matched device pairs are sized equally, therefore, we assumed in the sensitivity computation that the width W of the matched devices changes simultaneously. That is, the device widths W_1 and W_2 of transistors M_1 and M_2 are treated as one, and so to M_3 and M_4.

Fig. 3 shows the ac-sensitivity plots w.r.t. the three device sizes of M_1, M_3, and M_5. It shows that the matched transistor pair *M1-M2* has the largest ac-sensitivity in magnitude over the visible frequency range, while transistor *M5* has a prominent level transition in the visible frequency range. Comparing to the frequency response plots in Fig. 4 reveals that the middle point of the level transition is right at the dominant pole! The authors have analyzed this phenomenon and confirmed that this is generally true for any device parameters to which the poles or zeros are sensitive. But a detailed exposition in this respect is omitted due to the limited space.

The sensitivity plots are suggestive that increasing the device width of the matched pair *M1-M2* would move the magnitude curve upward to reach a higher dc gain and a larger f_t. On the other hand, sizing the transistor *M5* would shift the dominant pole to another desired location.

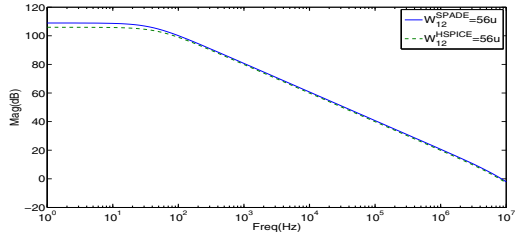


(a) Magnitude plots of ac-sensitivities.

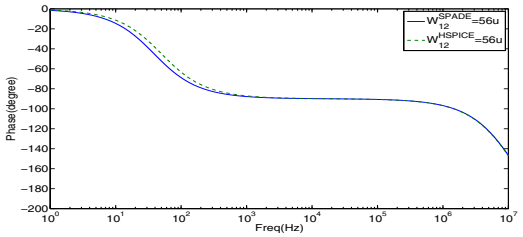


(b) Phase plots of ac-sensitivities.

Fig. 3: The ac-sensitivity plots for M1 to M5, with M1-M2 matched and M3-M4 matched.



(a) Magnitude plot.



(b) Phase plot.

Fig. 4: Comparison of ac responses at $W_{1,2} = 56\mu$ (solid line by GRASS and dashed line by HSPICE).

SPADE provides sizing bars in a graphical interface so that the user can interactively select a device size to slide while monitoring the change of the ac response curves. By sizing the width of the transistor pair *M1-M2* from 7μ to 56μ, we observed that both the unity-gain frequency f_t and the dc-gain met the specification. We compared the newly sized symbolic frequency response to that simulated by HSPICE. Fig. 4 shows that the symbolically estimated response after resizing (the solid line) closely approximate the accurate HSPICE result (the dashed line), indicating that the symbolic ac-sensitivity computed in the saturation region can be reused over a certain range of device sizes.

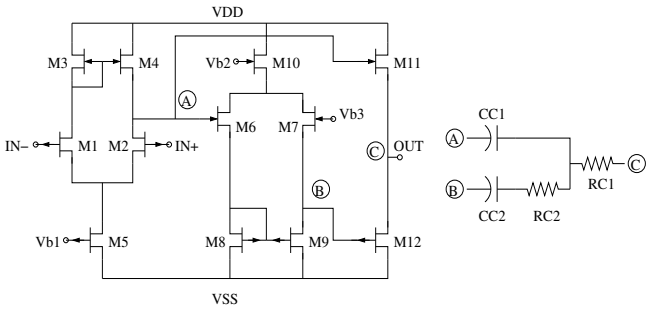
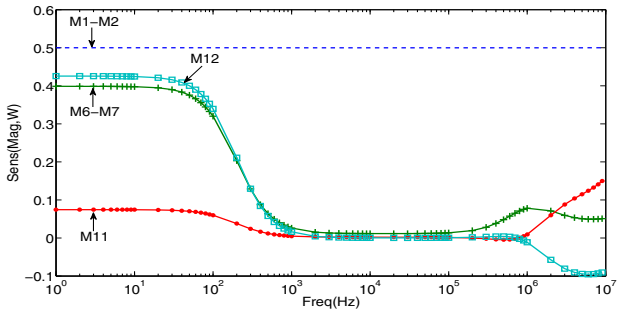
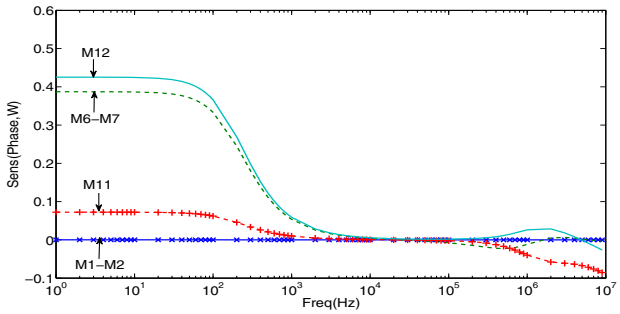


Fig. 5: A three-stage op-amp [14].



(a) Magnitude plots of ac-sensitivities.



(b) Phase plots of ac-sensitivities.

Fig. 6: Sensitivity of some selected transistors considering matching for the three-stage op-amp.

B. Design Case 2: A three-stage op-amp

The second example shown in Fig. 5 is a three-stage op-amp circuit studied in [14]; it contains 15 MOS transistors (including 3 transistors for voltage biassing not drawn.) The compensation device parameters were selected as *CC1 = 5pF, CC2 = 20pF, RC1 = 600 Ω, and RC2 = 5 Ω*. This example was chosen to demonstrate that the symbolic simulator GRASS is capable of analyzing practical analog circuits containing 10 to 20 transistors. If op-amps containing more transistors need to be analyzed, a hierarchical implementation should be used, which is to be reported elsewhere.

After an initial sizing, the ac-sensitivities to the selected six transistors M1-M2 (matched), M6-M7 (matched), M11, and M12 are plotted in Fig. 6. The ac-sensitivity of the input pair (*M1-M2*) stays nearly constant over the visible frequency range, which is analogous to what plotted in Fig. 3 for the input pair. The ac-sensitivity of the transistor pair *M6-M7* follows that of *M12*; both curves display clear level transitions in the band from 100 to 1,000 Hz, indicating that there exists a dominant pole in that band, and that pole is sensitive to the devices *M6-M7* and *M12*. In contrast, the transistor *M11* also has an ac-sensitivity level-shit at the pole location, but its sensitivity strength is much weaker than that of the devices *M6-M7* and *M12*.

IV. Conclusion

This paper has addressed the symbolic computation of ac-sensitivity to the semiconductor device sizes and investigated the potential applications of the ac-sensitivity visualization as an analog design aid. In contrast to the frequency response plots, where the device dependencies are not visible, the ac-sensitivity plots can reveal which devices are more relevant to the ac metrics (such as poles, zeros, bandwidth, unity-gain, phase margin, and gain margin, etc.) Therefore, with such a tool as presented in this paper, laborious analytical derivations can be minimized in design practice. The ac-sensitivity plots as given in the examples are highly informative to the designer, warranting the value of this research. In the future we would like to make such a design automation tool more automatic and more reliable.

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