Digital Integrated Circuits
A Design Perspective

Designing Combinational Logic Circuits

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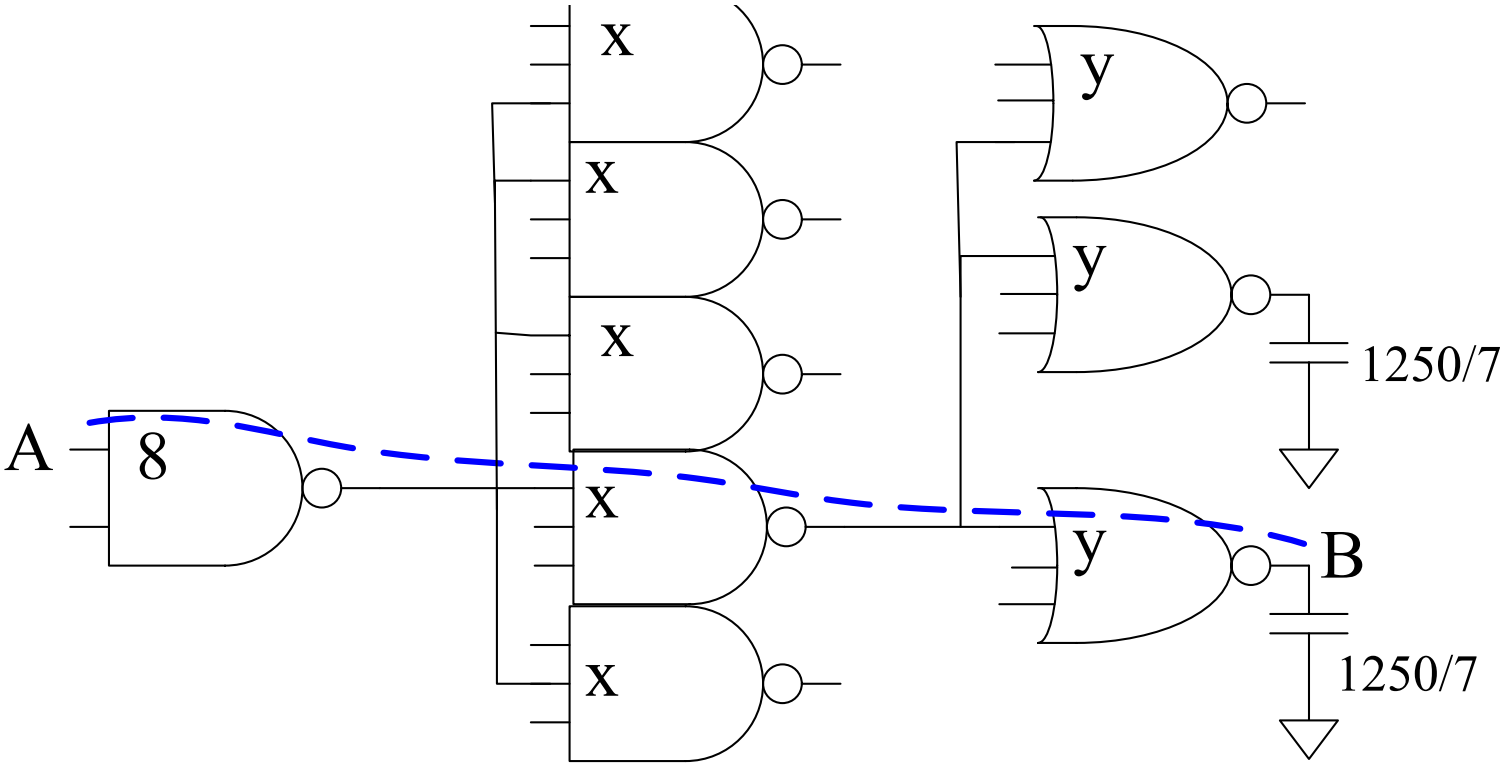
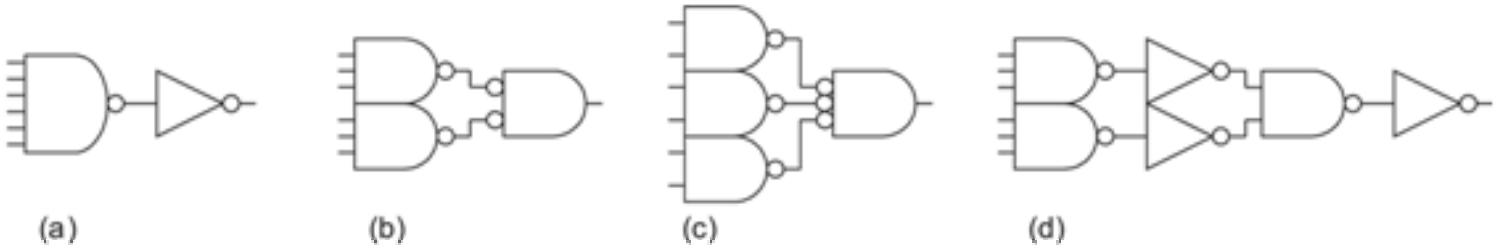
homework

- Sketch a 4-input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to a unit inverter.
  - Compute the rising and falling propagation delays(in terms of R and C) of the NAND gate driving h identical NAND gates using the ELMORE delay model
  - Compute the rising and falling contamination delays(in terms of R and C) of the NAND gate driving h identical NAND gates using the ELMORE delay model
  - If C=2fF/um and R=2.5kohm.um in a 180nm, what is the delay of a fanout-of-3 NAND gate?

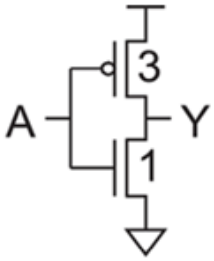
- Select gate sizes x and y for least delay from A to B



- Consider four designs of a 6-input AND gate shown in figure. Develop and expression for delay of each path if the path electrical effort is H. what design is fastest of H=1? For H=5? For H=20? Explain your conclusion intuitively

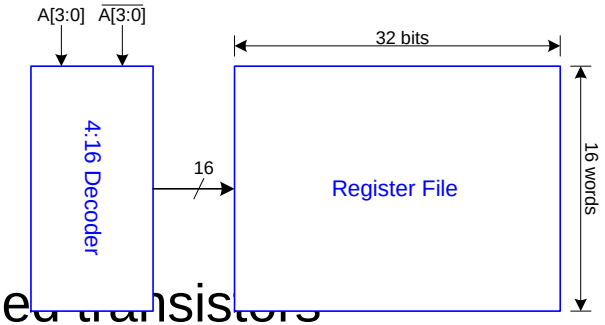


- Consider a process in which pMOS transistors have three times the effective resistance as nMOS transistors. A unit inverter with equal rising and falling delays in this process is shown in figure. Calculate the logical efforts of a 2-input NAND gate and a 2-input NOR gate if they are designed with equal rising and falling delays
- Generalize the model if the pMOS transistors have u times the effective resistance of nMOS transistors. Find a general expression for the logical efforts of a k-input NAND gate and a k-input NOR gate. As u increases, comment on the relative desirability of NANDs vs. NORs.



Example, Revisited

- Ben Bitdiddle is the memory designer for the Motoroil 68W86, an embedded automotive processor. Help Ben design the decoder for a register file.
- Decoder specifications:
  - 16 word register file
  - Each word is 64 bits wide
  - Each bit presents load of 3 unit-sized transistors
  - True and complementary address inputs A[3:0]
  - Each input may drive 10 unit-sized transistors
- Ben needs to decide:
  - How many stages to use?
  - How large should each gate be?
  - How fast can decoder operate?



- Find the worst-case ELMORE parasitic delay of an n-input NOR gate

- Design a 4-input footed dynamic NAND gate driving an electrical effort of 1. estimate the worst charge sharing noise as a fraction of Vdd assuming that diffusion capacitance on uncontacted nodes is about half of gate capacitance and on contacted nodes it equals gate capacitance.

- Design a k-input AND gate with DeMorgan's law using static CMOS inverters followed by a k-input pseudo-nMOS NOR,as shown in figure. Let each inverter be unit-sized. If the output load is an inverter of size H, determine the best transistor sizes in the NOR gate and estimate the average delay of the path