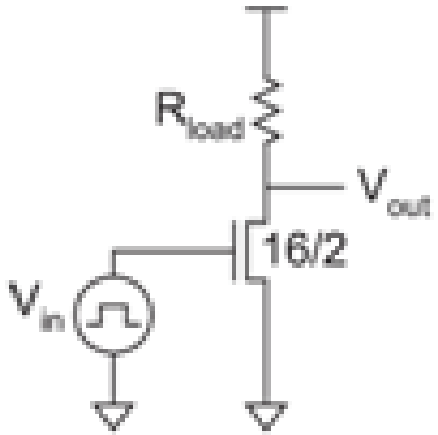
3.CMOS Inverter-homework

- 1. for a CMOS inverter, when the pMOS and nMOS are long-channel devices ,or when the supply voltage is low, velocity does not occur, under these circumstances,Vm(Vin=Vout)=?
- 2. for a long channel model, please analysis a first-order expression of the current as function of Vgs and Vds in the reistive operation of a pMOS transistor.

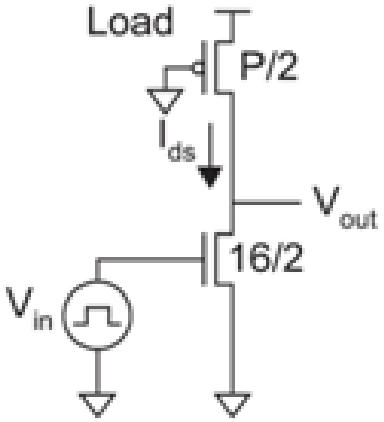
exercises

- 3.figure shows a generic nMOS inverter used a resistive load, assume VDD=1.8V, Rload=5K/10K/15K,please give a curve of I-V characteristics both resistive and nMOS



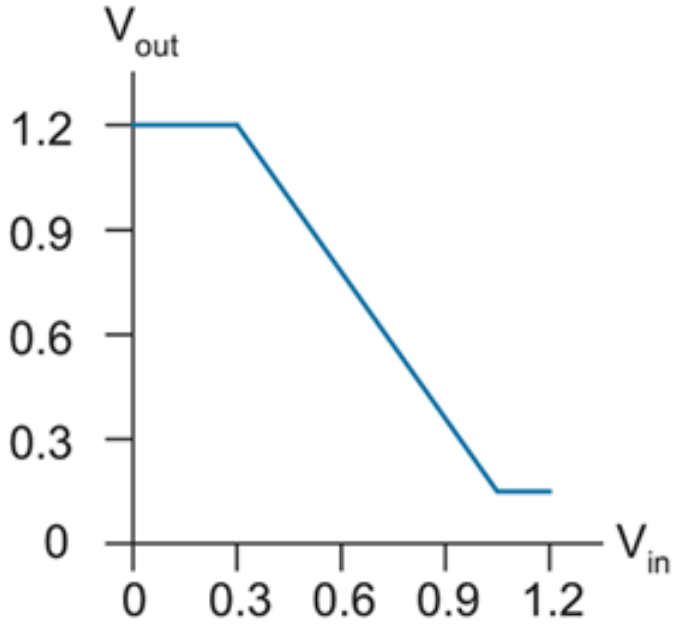
exercises

- 4.figure shows a generic nMOS inverter used a resistive load, assume VDD=1.8V, pMOS width=24/14/4,please give a curve of I-V characteristics both resistive and nMOS



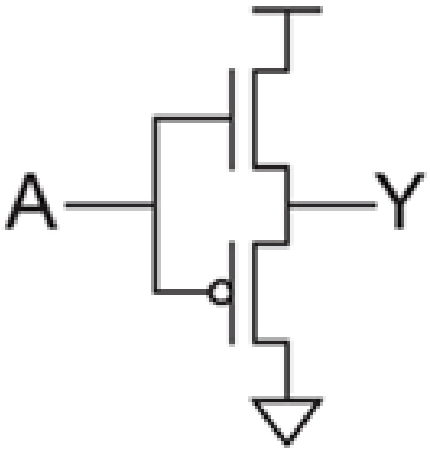
exercises

- 5.A novel inverter has the transfer characteristics shown in figure. What are the values of VIL,VIH,VOL, and VOH that give best noise margins? What are these high and low noise margin?



exercises

- 6.Graphically derive the transfer characteristics for this buffer.why is it a bad circuit idea

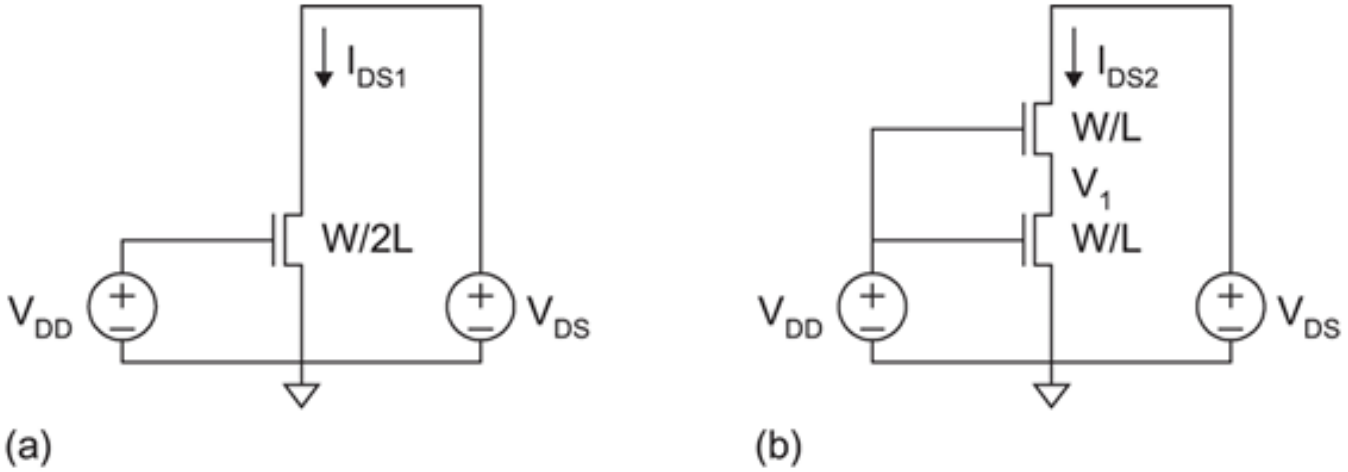


exercises

- 7.Consider an nMOS transistor in a 0.6um process with W/L=4/2r(i.e.,1.2/0.6um), in this process, the gate oxide thickness is 100A(1A=10^{-8}cm), $\varepsilon_{ox}=3.9\varepsilon_0=3.9*8.85*10\text{-}14F/cm$, the mobility of electrons is $350cm^2/V.s$, the threshold voltage is 0.7V. Plot I_{DS} vs. V_{DS} for V_{GS}=0,1,2,3,4,5V

exercises

- 8.Show that the current through two transistors in series is equal to the current through a single transistor of twice the length if the transistors are well described by the long-channel model. Specifically show that $I_{DS1}=I_{DS2}$ in figure when the transistors are in their linear region:$V_{DS}<V_{DD}-V_t$(this is also true in saturation).Hint:express the currents of the series transistors in terms of V_1 and solve for V_1



exercises

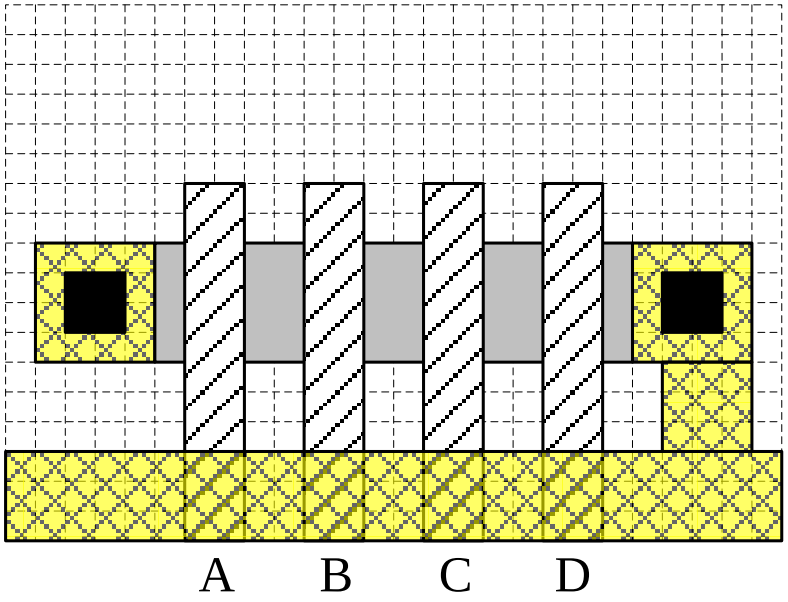
- 9.Calculate the diffusion parasitic CDB of the drain of a unit-sized contacted nMOS transistor in a 0.6um process when the drain is at 0 and at V_{DD}=5V. Assume the substrate is grounded. The transistor characteristics are CJ=0.42fF/um2,M_J=0.44,C_{JSW}=0.33fF/um ,M_{JSW}=0.12,and Ψ_0=0.98V at room temperature

exercises

- 10.Assume an inverter in the generic 0.25um CMOS technology designed with a PMOS-to-NMOS ratio of 6 and with the NMOS transistor minimum size(W=0.375um,L=0.25um,W/L=1.5)
- Please give the gain of VM, and VIL,VIH,NML,NMH, VTC curve

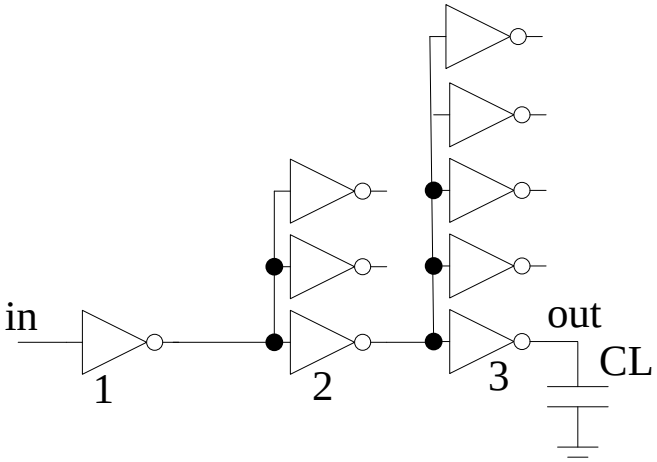
exercises

- 11.Calculating nMOS 1,2,3,4's AS(area of Source), AD(area of Drain),PS(perimeter of Source),PD (perimeter of Drain), assuming λ=0.25um, we use Keq=0.57,Keqsw=0.61,CJ=2fF,CJSW=0.28 for nMOS
- Calculating the internal capacitors between AB,BC,CD



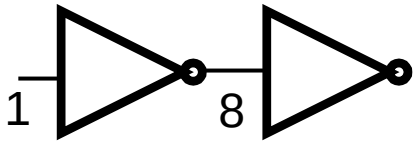
exercises

- 12.Determine the sizes of the inverters in the figure, such that the delay between nodes out and in is minimized, CL=64Cg1 is assumed



exercises

- 13.Calculate the internal capacitor between the two inverters using simple capacitor computing model, numbers show in the figure mean the nMOS width



exercises

- 14.Sizing a chain of inverters.
- a. In order to drive a large capacitance (CL = 20 pF) from a minimum size gate (with input capacitance Ci = 10fF), you decide to introduce a two-staged buffer as shown in Figure Assume that the propagation delay of a minimum size inverter is 70 ps. Also assume that the input capacitance of a gate is proportional to its size. Determine the sizing of the two additional buffer stages that will minimize the propagation delay.
- b. If you could add any number of stages to achieve the minimum delay, how many stages would you insert?What is the propagation delay in this case?

exercises

- c. Describe the advantages and disadvantages of the methods shown in (a) and (b).
- d. Determine a closed form expression for the power consumption in the circuit. Consider only gate capacitances in your analysis. What is the power consumption for a supply voltage of 2.5V and an activity factor of 1?