Chapter2-homework

- 2-1 For the circuit in Figure 0.2, *Vs* = 3.3 V. Assume *AD* = 12μm^2, φ_0 = 0.65 V, and *m* = 0.5. N_A = 2.5 E16 and N_D = 5 E15.
  - **a.** Find I_D and V_D.
  - **b.** Is the diode forward- or reverse-biased?
  - **c.** Find the depletion region width, *Wj*, of the diode.
  - **d.** Use the parallel-plate model to find the junction capacitance, *Cj*.
  - **e.** Set *Vs* = 1.5 V. Again using the parallel-plate model, explain qualitatively why *Cj* increases.

homework

- 2-2 Determine the NMOS and PMOS mode of operation (saturation, linear, or cutoff) and drain current ID for each of the biasing configurations given below. Verify with SPICE. Use the following transistor data: NMOS: k'_n = 115μA/V^2, V_{T0} = 0.43 V, λ= 0.06 V^{-1}, PMOS: k'_p = 30μA/V^2, V_{T0} = –0.4 V, λ= -0.1 V^{-1}. Assume (W/L) = 1.
  - a. NMOS: V_{GS} = 2.5 V, V_{DS} = 2.5 V. PMOS: V_{GS} = –0.5 V, V_{DS} = –1.25 V.
  - b. NMOS: V_{GS} = 3.3 V, V_{DS} = 2.2 V. PMOS: V_{GS} = –2.5 V, V_{DS} = –1.8 V.
  - c. NMOS: V_{GS} = 0.6 V, V_{DS} = 0.1 V. PMOS: V_{GS} = –2.5 V, V_{DS} = –0.7 V.

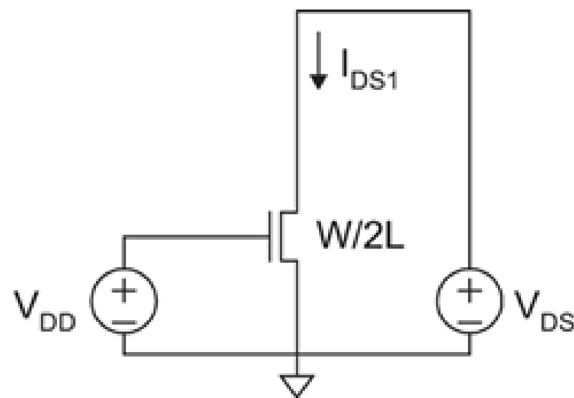
homework

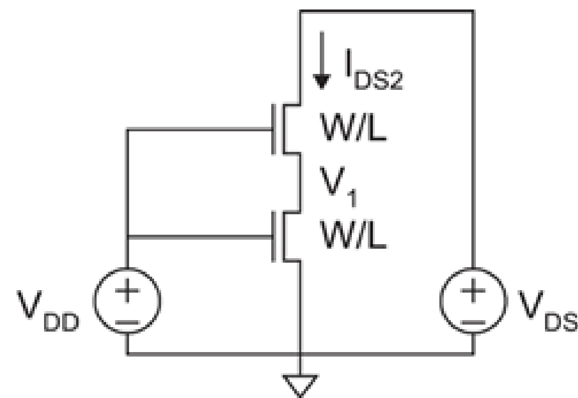
- 2-3 Given the data in Table 0.1 for a short channel NMOS transistor with V_{DSAT} = 0.6 V and k'=100 μA/V^2, calculate V_{T0}, γ, λ, 2|φ_f|, and W / L:

	V_{GS}	V_{DS}	V_{BS}	I_D (μA)
1	2.5	1.8	0	1812
2	2	1.8	0	1297
3	2	2.5	0	1361
4	2	1.8	–1	1146
5	2	1.8	-2	1039

homework

- 2-4 show that the current through two transistors in series is equal to the current through a single transistor of twice the length if the transistors are well described by the shockley mode. specifically show that $I_{DS1}=I_{DS2}$ in figure below when the transistors are in their linear region: $V_{DS}<V_{DD}-V_T$, $V_{DD}>V_T$(this is also true in saturation)





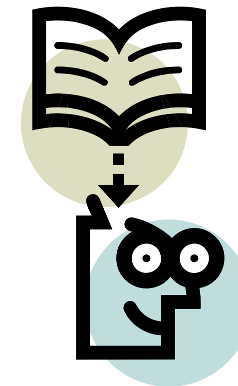
Homework

- 2-5 prove the formula

$$I_D = \frac{\mu_n C_{ox}}{1+\left({V_{DS}}/{L\xi_c}\right)} \frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$= \mu_n C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]\kappa(V_{DS})$$

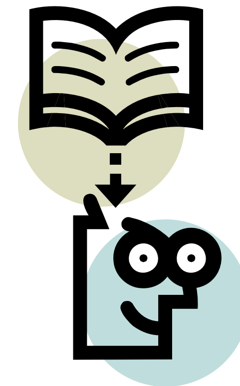
$$\kappa(V) = \frac{1}{1+{V}/{L\xi_c}}$$



Velocity Saturation

- 2-6 prove the formula

$$V_{DSAT} = \kappa(V_{GT})V_{GT}$$



homework

- 2-7 calculate the diffusion parasitic Cdb of the drain of a unit-sized contacted nMOS transistor in a 0.6um process when the drain is at 0 and at V_{DD}=5V. Assume the substrate is grounded. the transistor characteristics are :

  C_{J0}=0.42fF/um2,M_J=0.44,C_{JSW0}=0.33fF/um, M_{JSW}=0.12 and ψ_0=0.98V at room temperature

homework

- 2-8 consider the nMOS transistor in a 0.6um process with gate oxide thickness of 100A, the doping level is $N_A=2*10^{17}cm^{-3}$ and the nominal threshold voltage is 0.7V. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 4V instead of 0