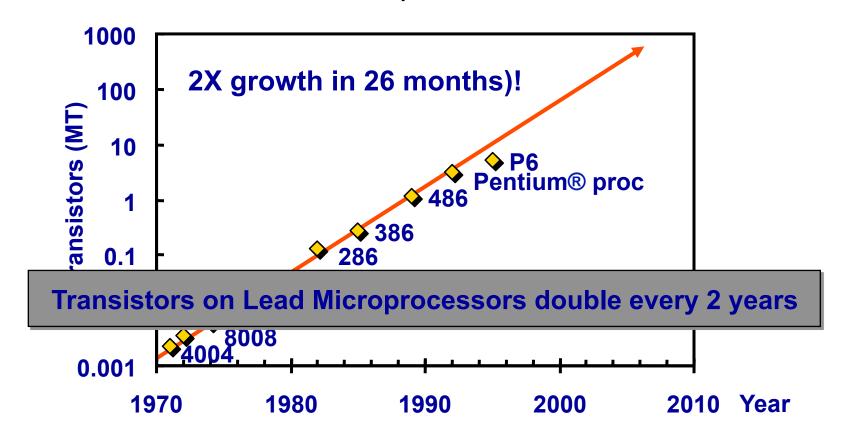
1.Introduction-Homework

 1-1Extrapolating the data from figure, predict the transistor count of a microprocessor in 2010



- 1-2 sketch a transistor-level schematic for a CMOS 4input NOR gate
- 1-3 sketch a transistor-level schematic for a single-stage CMOS logic gate for each of the following functions:

a)
$$Y = \overline{A + BC + D}$$

b)
$$Y = A + BCD$$

- 1-4 sketch a transistor-level schematic of a CMOS 2input XOR gate. You may assume you have both true and complementary versions of the inputs available
- 1-5 Sketch a stick diagram for a CMOS 3-input NOR gate
- 1-6 estimate the area of 1-5

- 1-7 sketch transistor-level schematic of the following logic functions. You may assume you have both true and complementary versions of the inputs available
 - a) 2:4 decoder defined by

$$Y0 = \overline{A0} \cdot \overline{A1}, Y1 = A0 \cdot \overline{A1}$$

 $Y2 = \overline{A0} \cdot A1, Y3 = A0 \cdot A1$

• b) 3:2 priority encoder defined by

$$Y0 = \overline{A0} \bullet (A1 + \overline{A2})$$
$$Y1 = \overline{A0} \bullet \overline{A1}$$

 1-8 Use a combination of CMOS gates(represented by their symbols) to generate the following functions from A, B, and C

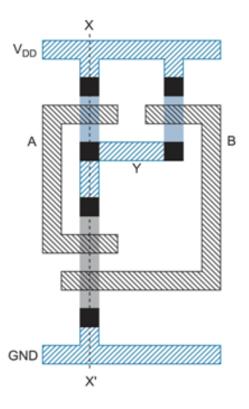
a)
$$Y = A(buffer)$$

b)
$$Y = A \overline{B} + \overline{A} B(XOR)$$

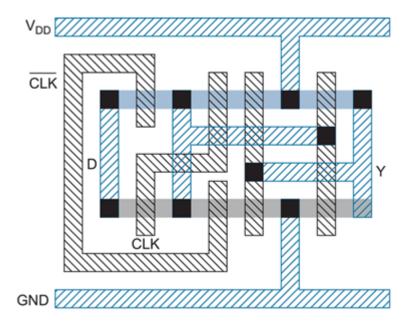
$$c) Y = AB + AB(XNOR)$$

$$d) Y = AB + BC + AC(SUM)$$

1-9 sketch a side view(cross section) of the gate from X to X'



1-10 translate the layout to circuit structure; estimate the area of the latch



homework

- 1-10 consider the design of a CMOS compound OR-AND-INVERT(OA21)gate computing $F = \overline{(A+B)C}$
 - Sketch a transistor-level schematic
 - Sketch a stick diagram
 - Estimate the area from the stick diagram
- 1-11 consider the design of a CMOS compound OR-AND-INVERT(OA22)gate computing $F = \overline{(A+B)(C+D)}$
 - Sketch a transistor-level schematic
 - Sketch a stick diagram
 - Estimate the area from the stick diagram